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To Enhanced the Performance of Multilevel Inverters with Reduced Harmonic Distortion using Eight Switching Devices

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ABSTRACT

A paper detailed investigation of the operating dynamics of a multilevel inverter is presented in this research using MATLAB simulation. The inverter architecture consists of eight switching units that combine unidirectional and bidirectional components. Two distinct designs are analysed to assess their performance characteristics: symmetrical and asymmetrical. Simulation yields the highest output voltages for the symmetrical configuration and Voltage for the asymmetrical design. Hence, the research employs Multiple Carrier Pulse Width Modulation (MCPWM) techniques to achieve this high voltage levels. The findings demonstrate the efficiency of the proposed multilayer inverter architecture and the strategic application of MCPWM to minimize harmonic distortions and provide high-voltage outputs.

Keywords: *Cascade Multilevel Inverter (CMI), Semi-conductors, Level Shifted, Total Harmonic Distortion (THD), Phase Disposition (IPD).*

1.0 Introduction

By adding cells in a cascade pattern, a multilevel inverter is able to provide an output voltage at a higher level and a waveform that is approximately sinusoidal [1]. As compared to the other two primary multilevel inverter topologies—the diode-clamped H-bridge and the flying-capacitor topologies—the cascade H-bridge has many advantages over its counterparts [2]. Typically, a single dc source and two switches are used in each leg of a cascade multilevel inverter. When all of the dc sources have the same magnitude, the resulting configuration is called a symmetrical configuration, but when they have different magnitudes, the resulting structure is called an asymmetrical configuration [3]. One of the key parameters in determining the price and efficacy of a power converter's cooling system is the converter's loss. While an asymmetrical layout allows for a greater range of voltages to be used in a given circuit, it comes with the significant drawback of putting a heavy load on all of the switches during operation [4].

In order to achieve a greater number of voltage levels, a cascade architecture multilevel inverter requires a greater number [5]. As the number of cells in a circuit grows, so does the number of switches linked to it, increasing the complexity of the circuit's design and operation. The modulation approach plays a crucial role in improving the efficiency of the new topology for CMI [6]. This study presents a CMI-based architecture with seventeen levels that uses the multi-channel power-wave management (MCPWM) approach. A CMI-based architecture with a decreased number of switches, as illustrated in fig.1, is used to provide an output voltage with seventeen discrete steps.

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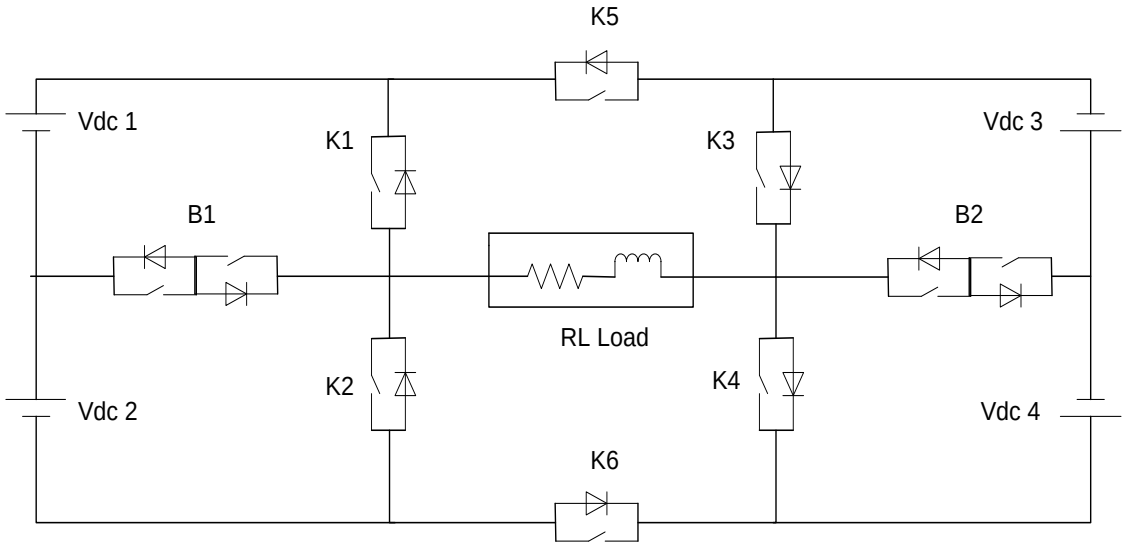
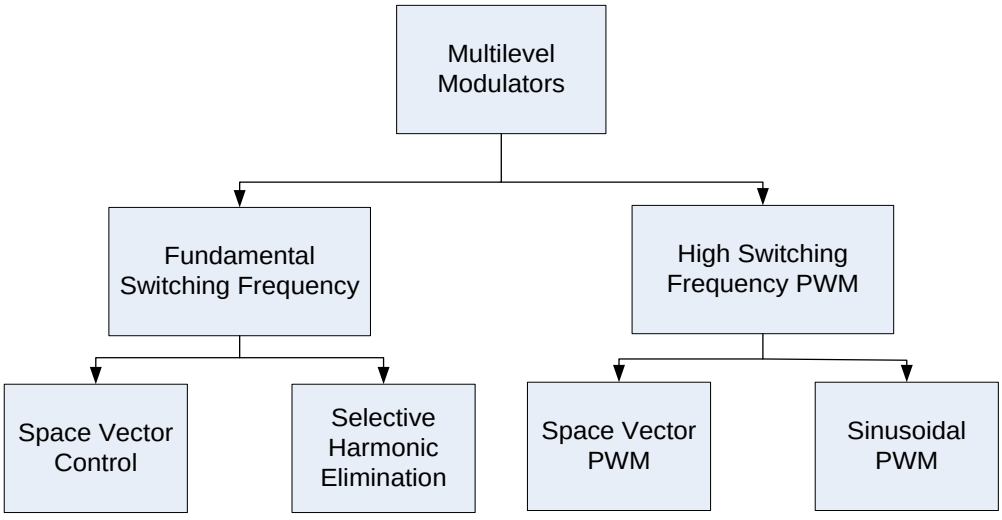
Figure 1: CMI based Strategy



2.0 Proposed Strategy

CMI, with its modular construction, is the most efficient design for multilevel inverters, but it has drawbacks as increasing the number of switching of system to increase the output voltage levels [7]. In order to address this shortcoming of CMI, a novel topology has been shown in which fewer switches are used than in the conventional cascade architecture of multilevel inverter.

Figure 2: Modulation Techniques Classification for CMI



2.1 Design the CMI strategy based circuit

As can be seen in Figure 1, this work introduces a cascade multilayer inverter based design that requires fewer switching components. In contrast to the traditional topology, which uses 32 switches to achieve the same number of levels (17), the given design requires just eight. All the switches brought about by the inductive load being used have likewise been outfitted with anti-parallel diodes in this topology. Vdc1, Vdc2, Vdc3, and Vdc4 are four different dc sources used at

both ends of the circuit. To get seventeen distinct states, an asymmetrical setup is used in which the left and right battery terminals' voltage ratings are maintained distinct. When all four batteries have the same voltage rating, this configuration is called a symmetrical arrangement, and it may provide nine different levels of output voltage.

2.2 Strategy methodology

The circuit looping technique is used to create different voltage levels in the circuitry shown in Figure 1. The operating process for this circuitry is defined in terms of the output voltage levels that need to be produced and the number of power semi-conducting components. The greatest voltage that this system can deliver voltages. various switching configurations are triggered for voltage level. With this design, the circuit must have seventeen switching states to provide the seventeen output voltage levels shown in Table 1. This configuration is used in both symmetrical and asymmetrical layouts. In an asymmetrical layout, The magnitude of each dc source in a symmetrical arrangement is the same, however the values found for the dc voltage sources on the left and right outer ends differ. One DC voltage source is on the left, while three are asymmetrically positioned on the right end. The functional differences between symmetrical and asymmetrical CMI designs are shown in Table 2. Together with the maximum output voltage that was reached, this table also includes the number of output voltages, switching devices, and DC sources utilized in the CMI-based system.

2.3 Loss Calculation of CMI

It is important to take extra care while creating the switching state of the circuit to ensure that all switches are subjected to an equal amount of voltage stress and that there are an equal proportion of switches in the on condition with each voltage level. Equations (1) and (2) may be used to get the peak and average conduction losses, respectively.

$$p_{on}(t) = |i_c(t)|(V_0 + R_{on}|i_c(t)|) \quad \ldots 1$$

$$p_{avg} = \frac{1}{2\pi}\int_0^T p_{on}\,(t)dt \quad \ldots 2$$

The on-state current i_c is related to the threshold voltage V_0 and the equivalent resistance R_{on} of semiconducting devices (t).

Because of the time it takes for switching devices to go from their off to them on states, energy is lost in the form of switching losses. The total of the diode's turn-on and turn-off losses is the switching loss; if the former is understood, the latter may be prevented. With equations (3), (4), and (5), respectively, one may decompose the energy dissipation associated with IGBT switching into losses during IGBT on, IGBT off, and diode off.

$$E_{on=\int_{t1}^{t2} v(t)*i(t)dt} \quad \ldots 3$$

$$E_{off=\int_{t3}^{t4} v(t)*i(t)dt} \quad \ldots 4$$

$$E_{rr=\int_{t5}^{t6} v_{rr(t)*i_{rr}}(t)dt} \quad \ldots 5$$

Power converter switching losses are sensitive to load situation, dc link inductance, gate circuit inductance, and temperature.

3.0 Modulation Techniques

Multilevel inverters, as shown in Fig. 2, employ a modulation technique based on the carrier wave switching frequency, which can be either constant or variable [9, 10]. It was hypothesised that

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phase shift carrier modulation would be more effective than SHE. MCPWM is favoured [11] because it provides less THD and a better output waveform, two of the most desirable characteristics of CMI. The output voltage waveform exhibits some degree of harmonics of lower order in the constant switching frequency technique, and it incurs less switching loss than the variable switching frequency approach [12]. It was hypothesised that phase shift carrier modulation would be more effective than SHE when the number of levels was large. Switching state redundancy is another strength of multilevel inverters, since it allows for versatile pattern design of switching, which is essential in space vector modulation systems.

Figure 3: Response Show the Level-shifted (IPD) Modulation

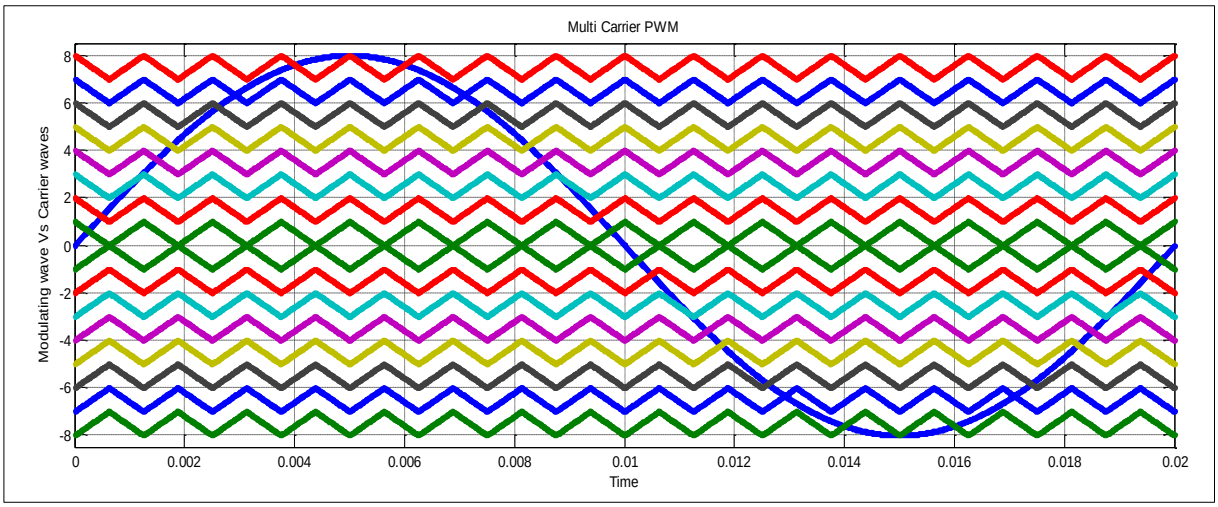

Table 1: Switching States for CMI based Topology

N_{level}	V_{out}	Switches (ON state)
1	0	K1, K3, K5
2	V_{dc}	K4, K6, B1
3	$2V_{dc}$	K1, K4, K6
4	$3V_{dc}$	K2, K6, B2
5	$4V_{dc}$	K6, B1, B2
6	$5V_{dc}$	K1, K6, B2
7	$6V_{dc}$	K2, K3, K6
8	$7V_{dc}$	K3, K6, B1
9	$8V_{dc}$	K1, K3, K6
10	$-V_{dc}$	K3, K5, B1
11	$-2V_{dc}$	K2, K3, K5
12	$-3V_{dc}$	K1, K5, B2
13	$-4V_{dc}$	K5, B1, B2
14	$-5V_{dc}$	K2, K5, B2
15	$-6V_{dc}$	K1, K4, K5
16	$-7V_{dc}$	K4, K5, B1
17	$-8V_{dc}$	K2, K4, K5

4.0 Simulation Result

Cascade multilevel inverter-based architecture is shown by simulating a multilevel inverter in MATLAB for both asymmetrical and symmetrical configurations (see fig. 1). This CMI structure may provide output voltage at seventeen distinct levels for an asymmetrical arrangement and nine different levels for a symmetrical design when employing the MCPWM (IPD) technique. Figures 4 and 5 depict the voltage output at various loads and unloading, with the latter showing nine levels. The highest output voltage of the seventeen settings is 200 volts, with nine settings offering 100 volts. This inverter will be used with a resistive-inductive type load at a frequency of 50 Hz. Fig. 6 displays the voltage and current produced by a seventeen-level inverter when it is fully loaded. Figures 7 and 8 demonstrate that for an inverter with seventeen levels of voltage regulation, the harmonic distortion of the output voltage is 6.25 percent, and for an inverter with nine levels of regulation, it is 21.83 percent.

Figure 4: Seventeen-level Output Voltage with Asymmetrical Condition

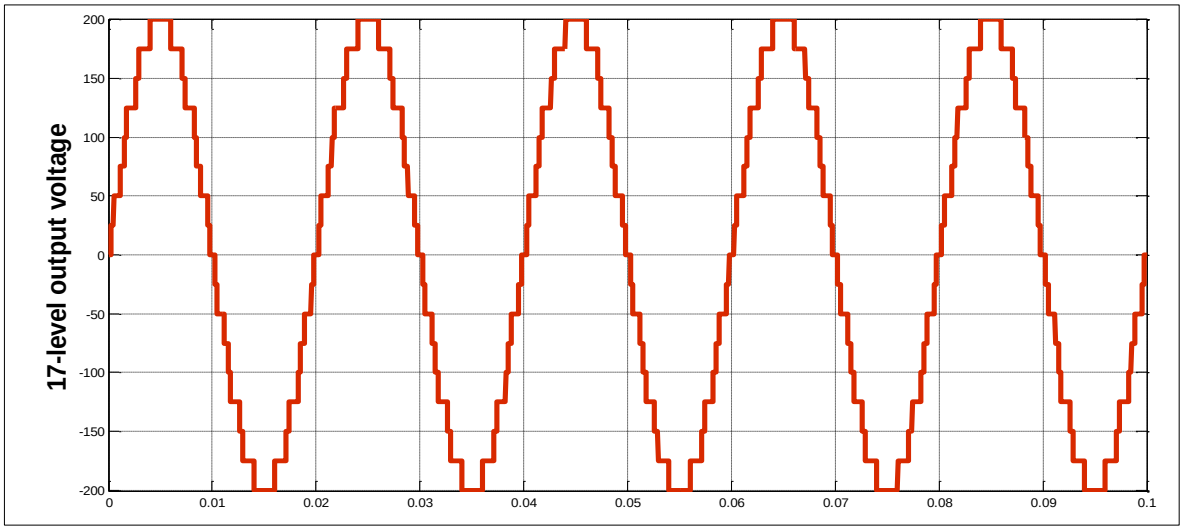

Figure 5: Response Show the Output Voltage with Symmetrical Condition

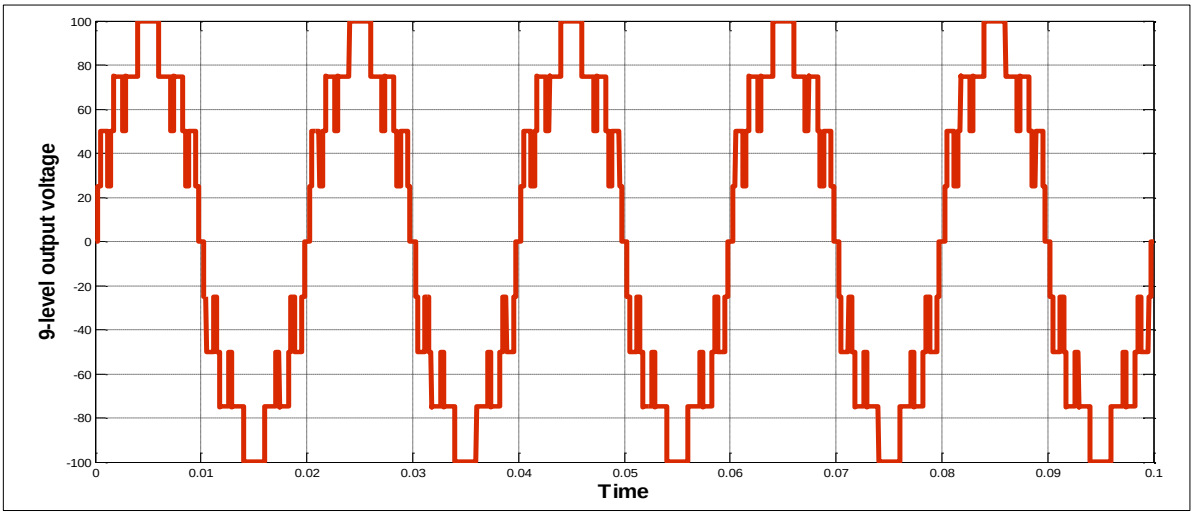

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Figure 6: Response Show the Output Voltage & Current at Various Load

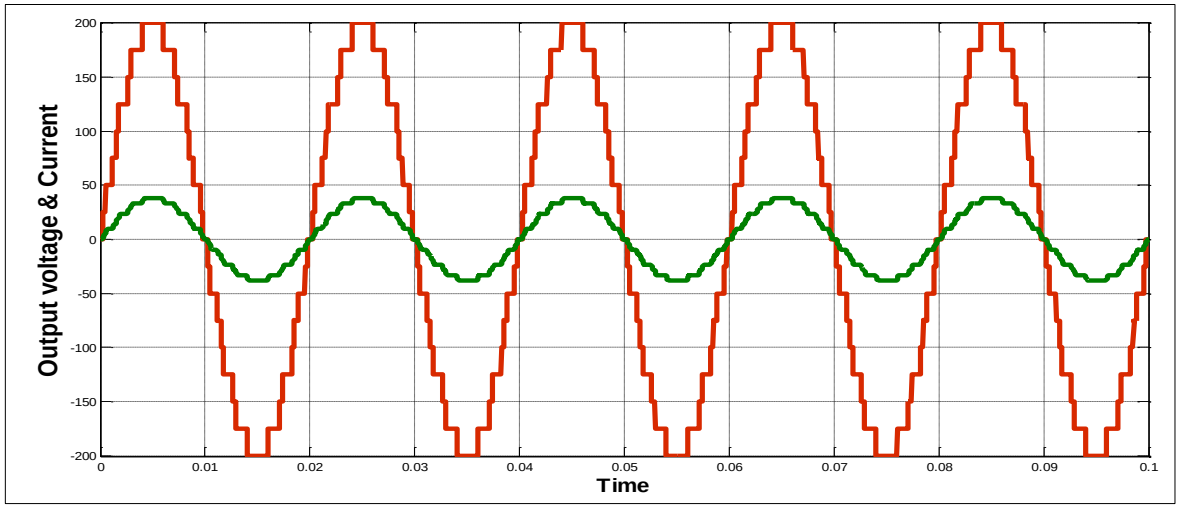
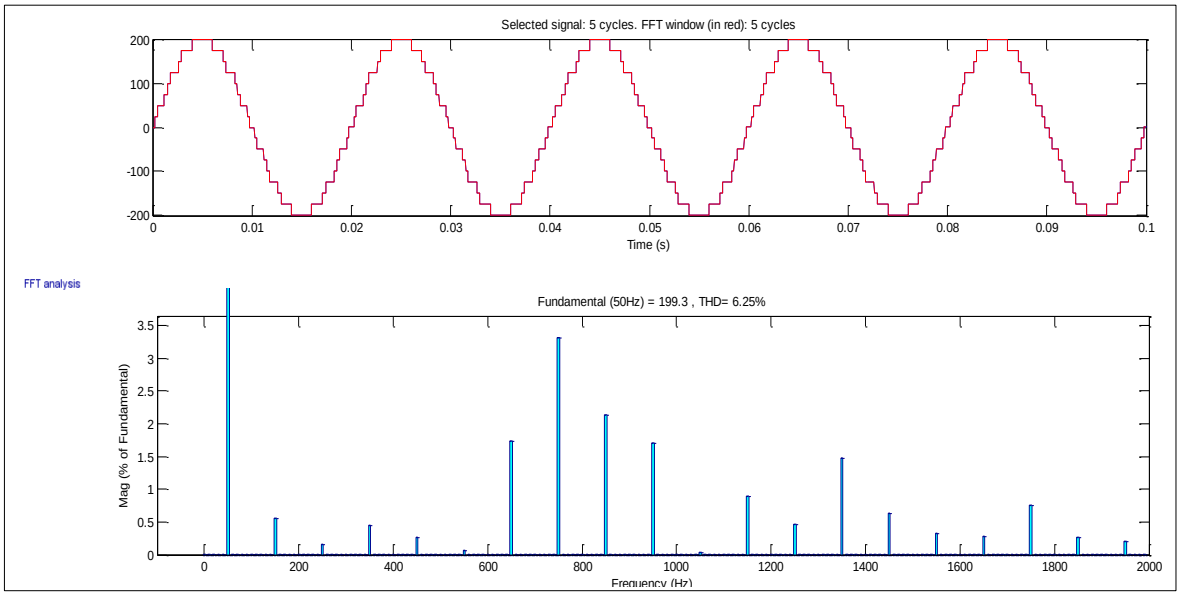


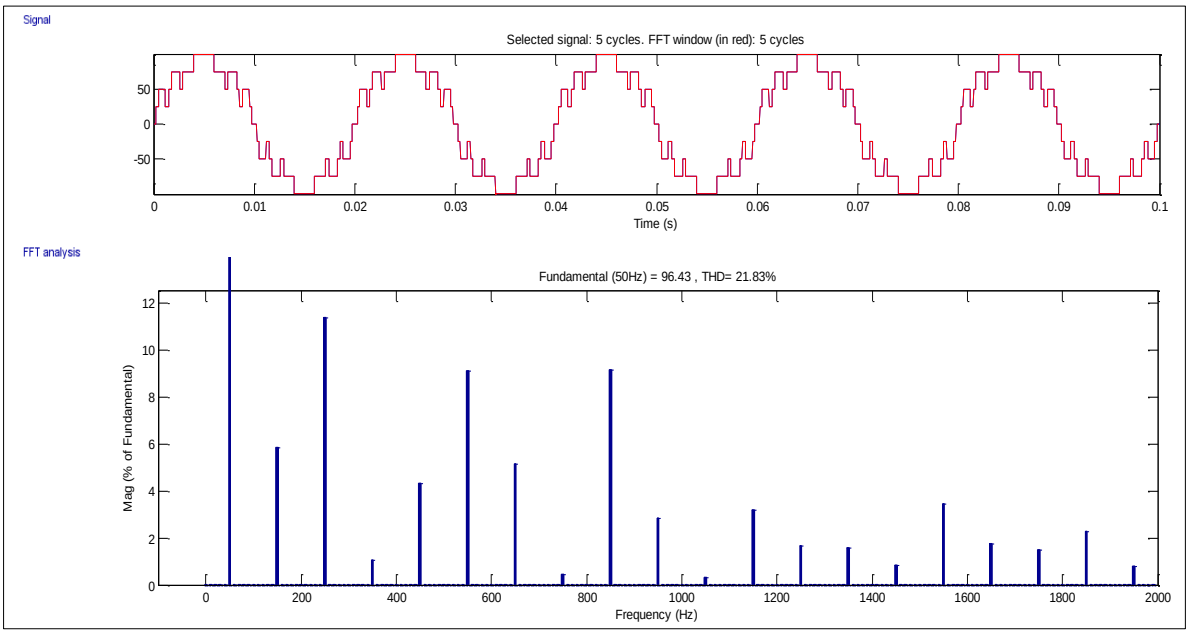
Figure 7: Response Show the THD of Output Voltage



5.0 Conclusion

The study on multilevel inverters since their inception in the late 1990s has seen significant advancements, encompassing various modifications ranging from novel topologies to sophisticated control mechanisms and modulation procedures. These modifications have primarily aimed at alleviating system burdens by minimizing switching components while concurrently improving the resolution of the output voltage. In this research, a particular multilevel inverter configuration employing eight switching devices has been thoroughly investigated, showcasing its capability to produce an output voltage spectrum comprising seventeen discrete levels. This achievement underscores the efficacy of the employed multi-carrier pulse width modulation technique in drastically mitigating harmonic distortion.

Figure 8: Response Show the THD of Output Voltage



The findings of this study contribute substantially to the ongoing efforts in optimizing multilevel inverter systems, promising enhanced performance and efficiency in various applications such as renewable energy systems, motor drives, and power electronics. As such, further exploration and refinement of multilevel inverter technologies hold great potential for advancing the field of power electronics and facilitating the transition towards more sustainable and efficient energy utilization paradigms.

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