Journal of Futuristic Sciences and Applications
Vol. 6(2), Jul-Dec 2023, pp. 42-47
doi: 10.51976/jfsa.622307
www.gla.ac.in/journals/jfsa

Design and Analysis of Single Bit Cache Memory Architecture

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ABSTRACT

Today's computer environment places a high value on energy efficiency, making cache memory design and optimization crucial. Cache memory is designed to decrease data access latency and enhance system performance by acting as a high-speed buffer between the processor and main memory. Traditional cache designs, on the other hand, can have large power consumption, which is undesirable in systems with tight power limits or in devices that run on batteries. This work investigates six-transistor static RAM cells with voltage latch sensing amplifiers. The cache memory design for the single-bit architecture has been studied at different resistance values. The stability of the design was assessed using Monte Carlo simulation and Process Corner simulation. As the resistance value increases, a single-bit static random access memory cell latch sensing amplifier architecture consumes less energy.

Keywords: *Voltage latch sense amplifier (VLSA), write driver circuit (WDC), latchsense amplifier (LSA), six transistorsstatic random-access memory (STSRAM).*

1.0 Introduction

The three primary types of computer memory in use today are basic memory, cache memory, and register data [1-3]. Large-scale integrated circuits, or STSRAM technology, are frequently used by businesses to speed up procedures. Structured random-access memory (SRAM), a crucial memory component for processing data, typically makes up cache memory. This is an important factor to consider while considering STSRAM's potential growth. Even when the power is down, STSTRAM enables anyone with physical access to the device to view the data [4-7]. Due to its connection to the data line in a STSRAM, the LSA is frequently disregarded. LSA monitors the voltage on each bit line, and the total voltage swing as each bit line is read. Swing voltage cannot be used to record or measure data. It will store "0" or "1" in place of "0" or "1." As the VLSI industry grows, embedded systems and battery-powered mobile devices are taking on more significance [8-10]. Cache memory takes up between 60 and 70 percent of the chip's area in a single-bit architecture. When the number of chips in use rises quickly, CPU speed falls [8-10]. The business world is creating a low-speed, low-power memory circuit to keep up with VLSI's developments. A million transistors can alter a single device's failure rate. It is anticipated that cache memory in high-performance microprocessors will increase until it uses more than half the transistors. Due to its great dependability and stability, STSRAM is frequently used for on-chip storage in noisy situations. Since all SRAMC cells are the same size, the system can use any of them. It is common practice to estimate a system's time and power requirements using the LSA setup [11-14].

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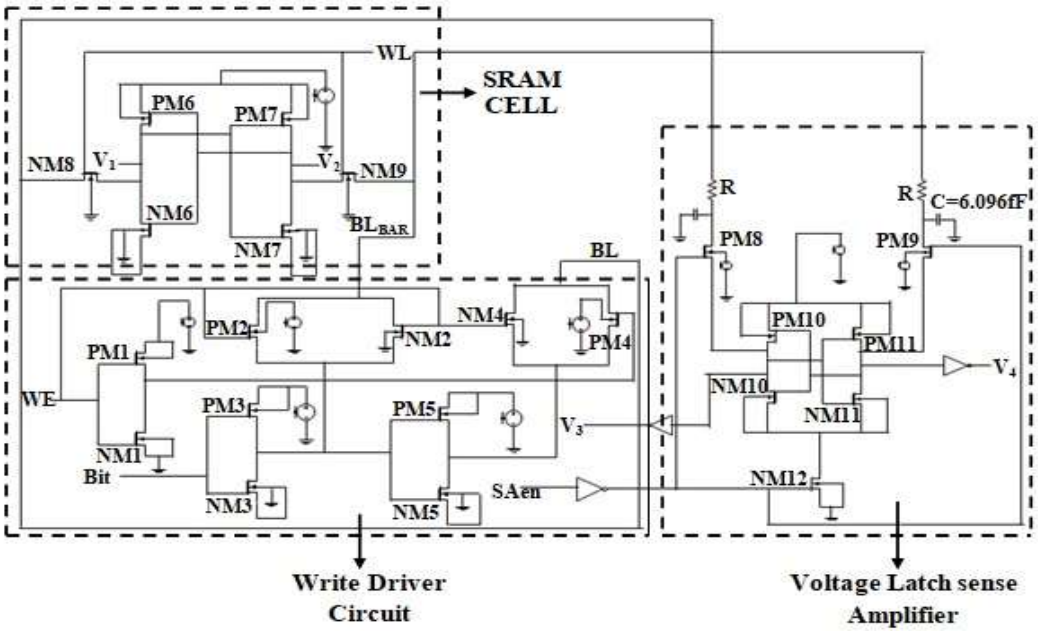
2.0 Design of Cache Memory for Single Bit Architecture

Here, designers discussed the cache memory's single-bit design in Figure 1. WDC, STSRAM, and LSA are workable solutions in a single-bit cache memory architecture.

Figure 1: Design of Cache Memory for Single Bit Architecture



2.1 Circuit of write driver

It is dependable and a great option for tasks needing low voltage and power. A two-way latch is used to store each bit in a circuit [15,16].

Figure 2: Write Driver Circuit Schematic

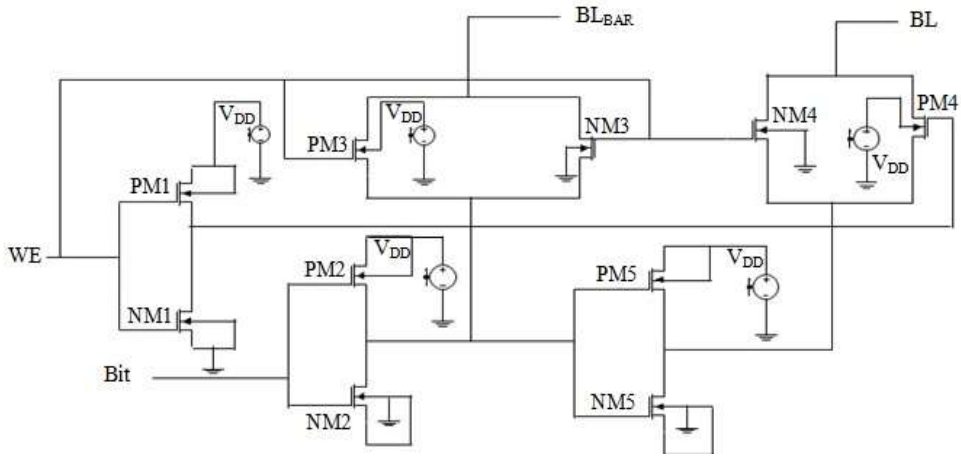


Figure 2 depicts the NM3 and NM4 driving transistors for a STSRAM cell. One of the transistors in this circuit is the driving transistor. These bit lines widen the noise margin. Researchers can calculate how much voltage can fluctuate by using a differential circuit. As long as the present

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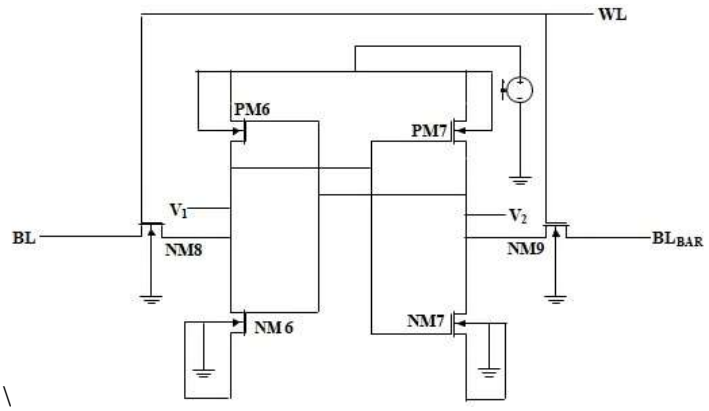
power cycle lasts, the logical state won't change. The DRAMC should not be refilled at this time [17]. When creating a STSRAM, the transistor's size is crucial.

2.2 Six transistor static random-access memory cell

It's perfect for jobs that don't call for a lot of power or voltage. A circuit that can latch in both directions is used to store each bit. The STSRAM cell in Figure 3 has two pull-ups, two drivers, and two pull-downs [18-20]. These bit lines widen the noise margin. A differential circuit can be used to compute the voltage swings that can be measured. The logical state of this power cycle is either 0 or 1. The DRAMC does not, however, need to be changed as a result of this. When designing a STSRAM, the size of the transistors is crucial [21].

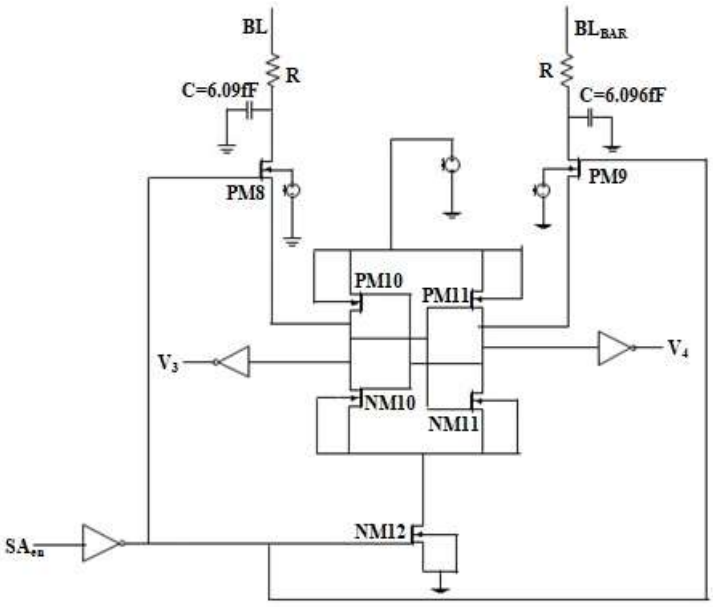
Figure 3: Six Transistor Static Random Access Memory Cell Schematic



2.3 Voltage latch sense amplifier

Figure 4 depicts the schematics for the voltage latch detecting amplifier in this instance. In this design, the nodes are charged in advance via bit-lines.

Figure 4: Schematics of Voltage Latch Sense Amplifier



The circuit's building blocks, the nodes, manage the input bit lines. When the word line is lifted, the amplifier sensor fires, but PM8 and PM9 are not engaged. The voltage differential impacts the random bit voltage in the internal nodes of the LSA between the bit lines. When the LSA SAEN signal is claimed, the greater voltage difference between inverters boosts maximum swing power [22–25].

3.0 Result Analysis

Figure 5 depicts a simulation of the cache memory using a single-bit design. Figure 6 displays the outcomes of a Monte Carlo simulation of the cache memory setup for a single-bit architecture.

Figure 5: Output Waveform of VLSA

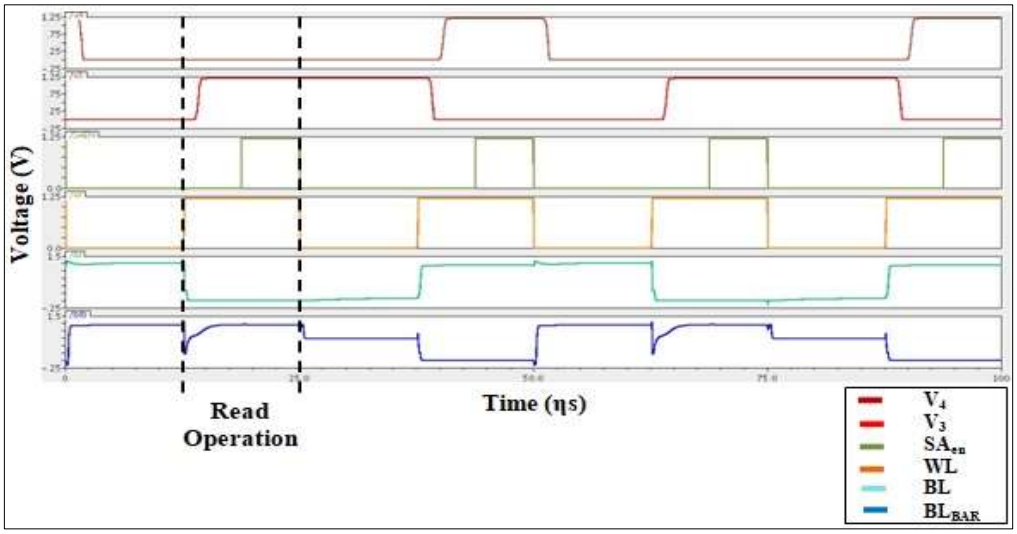


Figure 6: Process Corner Simulation

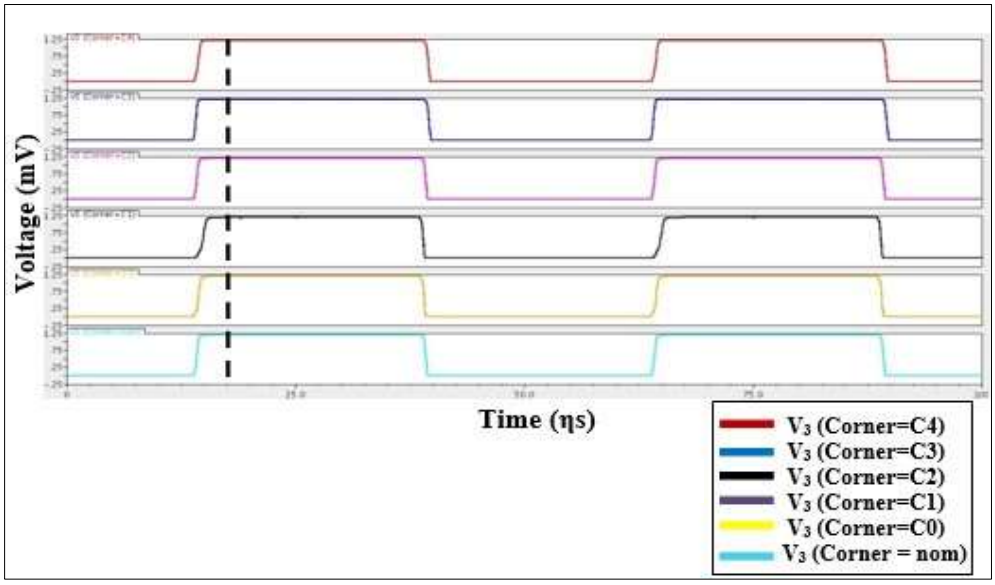


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Figure 7: Monte Carlo Simulation

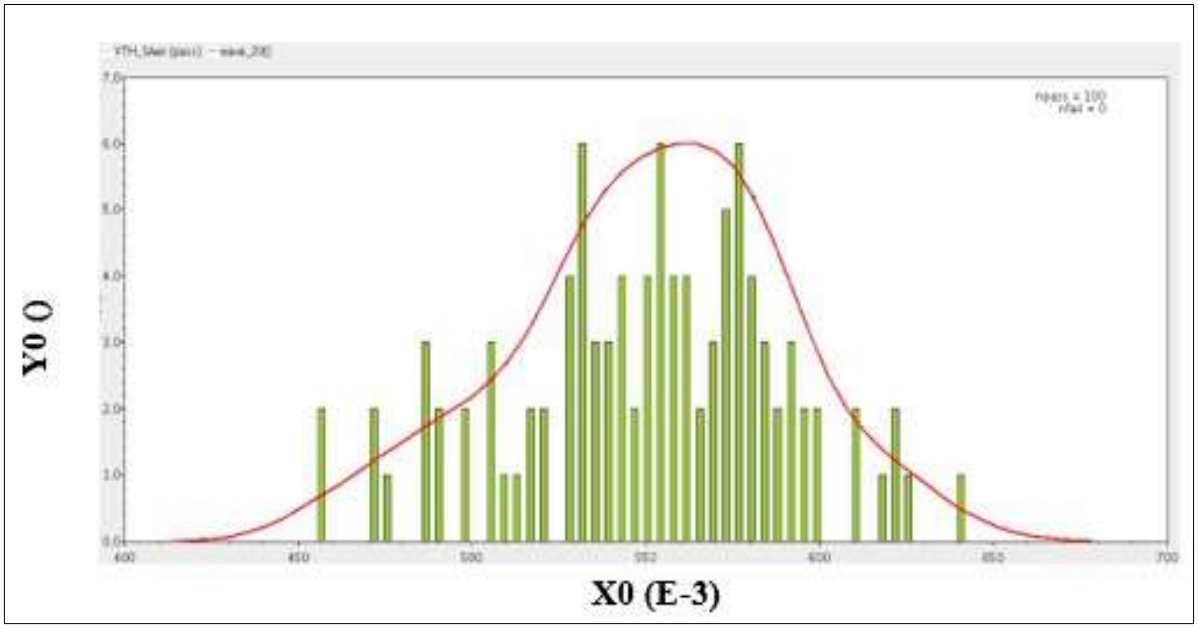

Table: 1 shows that when resistance increases, power consumption falls.

Table 1: Analysis of Single Bit SRAMC VLSA Design's Different Parameters

S. No.	Parameters	Delay in Sensing	Number of Transistors	Consumption of Power
1.	R=42.3Ω	25.78ηs	30	40.21μW
2.	R=42.3KΩ	25.78ηs	30	20.89μW

4.0 Conclusion

Cache memory is designed to decrease data access latency and enhance system performance by acting as a high-speed buffer between the processor and main memory. The purpose of this study is to investigate the design principles, benefits, and potential drawbacks of single-bit architecture in low-power cache memory systems. By understanding the complexity of this design philosophy, we may look into ways to make computing systems more energy-efficient without compromising performance**.**The different resistance levels of the single-bit cache memory structure are used to investigate these architectural elements. Monte Carlo and corner simulation have also been used to analyze the cache memory design for a single-bit architectural process. According to a study, single-bit cache memory consumes more power as resistance rises. In the future, this work might benefit from the use of arrays.

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