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Analysis of 6T SRAM Cell in Different Technologies

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ABSTRACT

An important component of embedded cache memory of handheld digital devices is Static Random Access Memory (SRAM). It has become major data storage device due to its large storage density and less access time. The demand of low voltage low power SRAM has been raised by the exponential growth of low power digital devices. At low voltage operation of any device, the noise margin is another parameter that needs attention. This paper gives the design and implementation of 6T SRAM cell in 180nm and 90nm standard CMOS process technology. The simulation has been performed in Cadence Virtuoso environment. The performance analysis of SRAM cell has been evaluated in terms of Static Noise Margin (SNM).

Keywords: *Static Random Access Memory; Circuit; Noise Margin.*

1.0 Introduction

Static Random Access Memory (SRAM) is a static memory cell which is being used in various electronic devices. It is faster as compared to other memory cells [1] and even consumes lesser power and is not required to be refreshed periodically. Hence, SRAM is the most popular memory cell among VLSI designers. Different types of SRAM cells are available in market like 6T SRAM cell, 7T SRAM cell, 8T SRAM cell, 9T SRAM cell and many more.

The most common SRAM cell used in digital system is the 6T SRAM cell. It stores 1-bit of data. The bit stays in the RAM if power is supplied. In this paper, design and performance analysis of a 6T SRAM cell has been discussed. Performance analysis is carried out by using Cadence Virtuoso in 180nm CMOS and 90nm CMOS1v and CMOS2v technologies. A basic 6T SRAM cell has two inverters connected back to back. Fig. 1 shows the basic structure of a 6T SRAM memory cell [2].

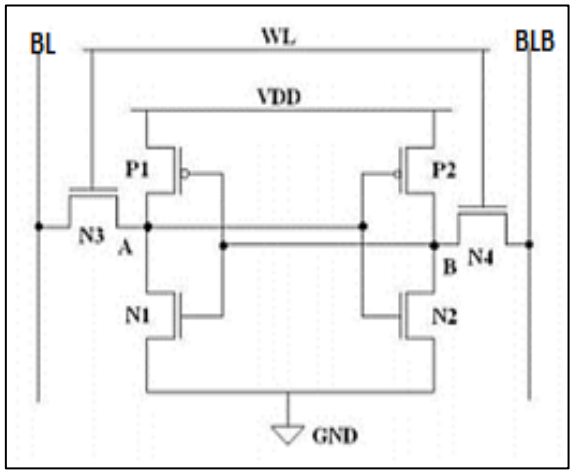
The data that is to be stored, is latched in these two inverters. Write operation is the process of storing a data, and Read operation is the process of recovering the data.

The contents in a SRAM cell are uploaded in the Write operation, while Read operation is used for fetching the contents. Sense circuits are used for the read operation which sense BL and BLB data line before discharging it completely [3-4].

2.0 Power Dissipation

Power dissipation in CMOS circuits is categorized in two types i.e. dynamic power and static power. It is the rate of energy which is consumed from the source and converted into heat. The switching behavior of the transistor results in dynamic power, which happens because of changing

Fig 1: 6T SRAM Cell



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and discharging of load capacitance. Static power dissipation is due to the leakage current produced continuously from the power supply. It can be minimized by various techniques; low power supply voltage is the most widely used technique to achieve lower dissipation of power. When low supply voltage is applied to the SRAM, the battery life gets improved. The power dissipation produces less heat. But it has been observed that SRAM stability and delay are affected when we decrease supply voltage [6]. Sub threshold leakage, gate induced drain current, drain induced barrier lowering, gate oxide tunneling, hot carrier effect are some factors which are responsible for leakage current [6].

3.0 Different Circuit Approaches

The conventional SRAM design has six transistors which consumes more power and has less stability for read operation [1]. Ajoy CA et al. [1] have reduced power consumption using low power techniques.

They used Cadence software to draw the schematic and to analyze static noise margin. The novel SRAM proposed by Ajoy C A et al. [1] provides minimum power consumption. Abhishek Agal et al. [4] evaluated SNM of existing 6T CMOS SRAM cell in 90nm and 180nm technologies.

4.0 6T SRAM Cell

The 6T SRAM cell (Fig. 1) consists of 6 MOSFETs where 4 transistors are coupled as CMOS inverter, here bit is stored as 1 or 0 and other two transistors control the SRAM cell by bit line, acting as pass transistors. The SRAM cell can be accessed when WL (word line) is high.

Following MOSFETs have been used in this work:

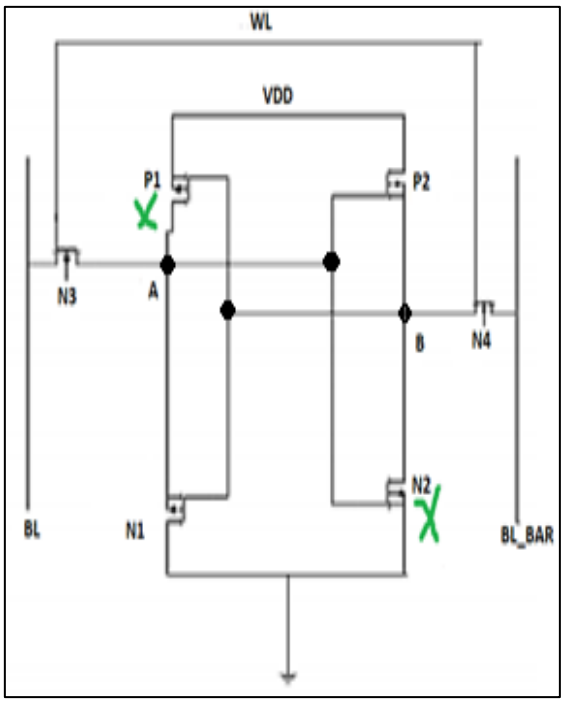
- mos – 1.8V nominal Vt NMOS and PMOS transistor
- mos1v - 1.2V nominal Vt NMOS and PMOS transistor
- mos2v – 2.5V nominal Vt NMOS and PMOS transistor

4.1 Standby mode

WL is 0 in standby mode in which the two pass transistors N3 and N4 are off and the SRAM cell cannot be accessed, and the contents of coupled transistors remain unchanged if supply voltage exists.

4.2 Read mode

Fig 2: Read Operation



The data read operation of SRAM is shown in Fig.2. WL has been selected in read mode which enables the two pass transistors N3 and N4, which are connected to the bit lines. The value stored at node A and node B are transferred to the bit lines now. First assuming 0 has been stored at node A, so BL will discharge through N3 and N1 transistors and the BL_BAR is pulled up through P2 to VDD. P1 and N2 transistors are turned off in this mode of operation but the transistors N1 and P2 are operate in linear mode.

4.3 Write mode

The write operation of 6T SRAM is shown in Fig. 3. To write something in SRAM either BL_BAR or BL are discharged to ground. BL is charged to Vdd and BL_BAR is discharged through ground when logic 1 needs to be written. BL_BAR is charged to Vdd and BL is discharged through ground when logic 0 needs to be written.

WL is made active if data is to be written in to the cell. Assume that 0 is stored at node A, and a 1 is to be written; 1 logic is given to BL line, which starts charging node A through N3 transistor. Thus, N2 is turned ON and the output of inverter P2-N2 (node B) starts to discharge, which turns ON P1. Thus, now the value 1 is written on node A.

5.0 Result Analysis

5.1 6T SRAM Cell in 180nm and 90nm technology cell design

In this work, 6T SRAM cell has been designed in 180nm and 90nm using Cadence Virtuoso tool which are shown in Fig. 4 and Fig. 5

Fig 3: Write Operation

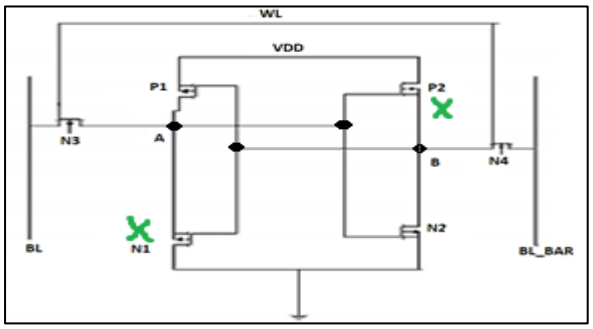


Fig 4: 6T SRAM Schematic in 180nm

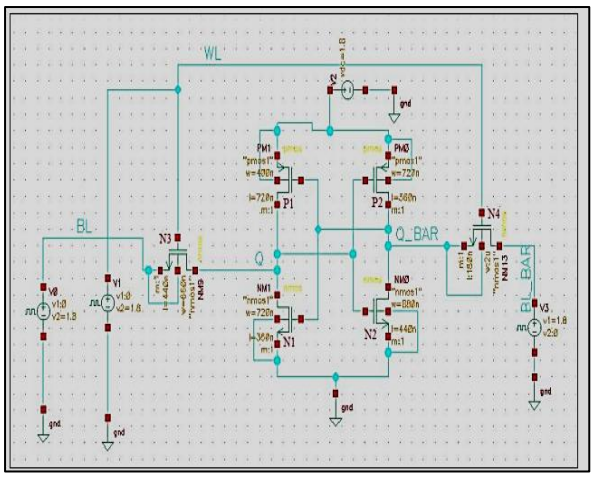
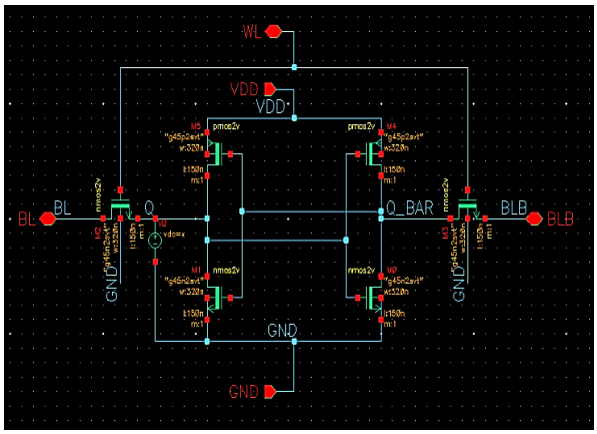


Fig 5: 6T SRAM Schematic in 90nm



5.2 Static noise margin (SNM)

One of the most important parameters for memory design is Static Noise Margin (SNM). It includes both read and write margin. The SNM has been achieved by DC analysis. SNM is shown in Figures 6-8 for various technologies. Table 3 shows the comparison of SNM in various technologies.

Fig 6: SNM Graph

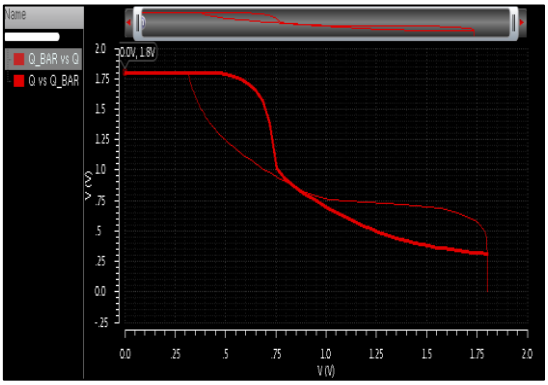


Fig 7: SNM Graph for 6T SRAM Using Nmos1v 90 nm

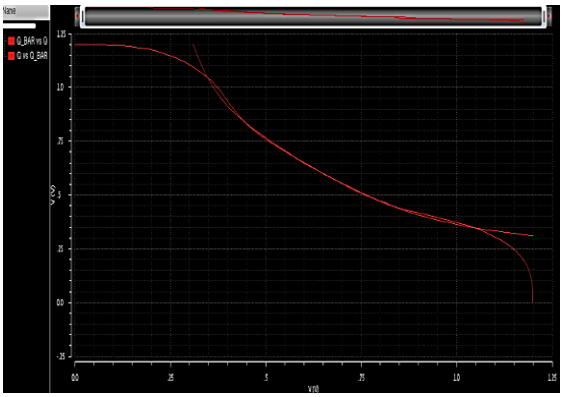


Fig 8: SNM Graph for 6T RAM Using Nmos2v 90 nm

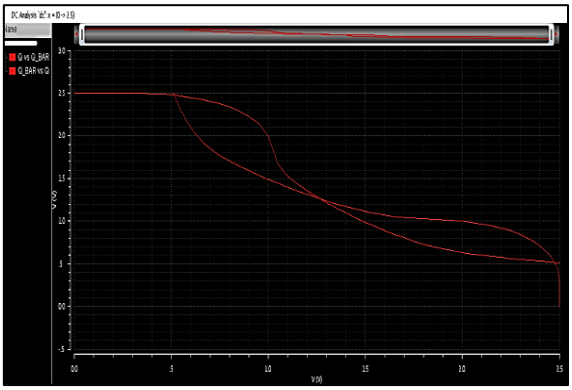


Table 3: Comparison of SNM in Various Technologies

Technology	SNM for read operation	SNM for write operation
mos 180nm	0.35V	0.31V
Mos2v 180 nm	0.25V	0.26V
mos 90nm	0.17V	0.07V
Mos2v 90 nm	0.15V	0.05V

6.0 Conclusions

6T SRAM cell has been designed in this work for 180nm and 90nm technologies. Cadence Virtuoso tool has been used for design and simulation. Static Noise Margin has been estimated for SRAM using nmos1V and nmos2V cells in both 180nm and 90nm technologies. As predicted, SNM gets worse with shrinking technologies; also, it has been observed that CMOS 1v has better SNM as compared to CMOS 2v transistors.

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