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DC Analysis and Inference of Noise Margins for FINFET Inverters

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ABSTRACT

As the devices are shrinking day by day, conventionally used planar transistor or MOSFETs seem to be insufficient. MOSFET has been into use in the industry since a long time. But the continuous need to minimize the channel length has been an issue with MOSFET. This problem can be solved by FinFET. As the channel region is surrounded by the gate from three sides in FinFET, it has a better control over the flow of electrons and thus the channel length can be altered or minimized. Noise margin is among the important parameters for determining the stability of a digital circuit. Hence, to be certain that the digital circuit is working properly, one must take into consideration stability parameters like noise margin. In this paper, we have compared the noise margins of different types of FinFET inverters.

Keywords: *Noise Margin; Inverters; Transistor.*

1.0 Introduction

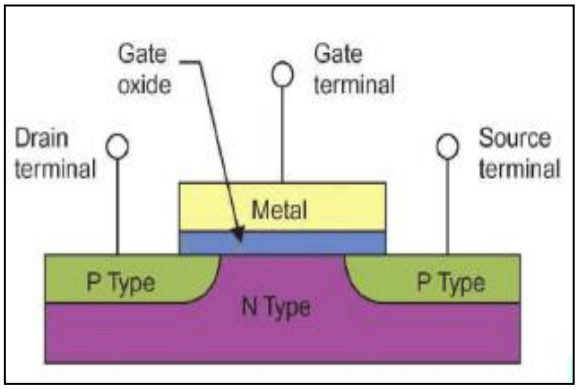
The metal oxide field effect transistor or MOSFET is the fundamental element used in integrated circuits as it is feasible for large scale productions. Other transistors were also used but are typically kept for high performance applications, BJT (bipolar junction transistor) is one of such transistors. Fin Field Effect Transistor or FinFET has slight changes in its design and architecture from MOSFET. In traditional MOSFET structures, a conducting region is built under the gate electrode in the silicon region when in on state. MOSFET has a planar or two-dimensional structure.

Figure 1 shows MOSFET having silicon substrate as n-type, heavily doped drain and sourse regions which are p-type and the gate terminal at the top. The channel is created in the region in between the drain and the source.

Because of increased leaks and process variations along with narrowing of the dimensions of the device, CMOS technology is facing challenges these days. Even with advanced manufacturing techniques, the bulk CMOS scalability remains restricted because of increased leakage and short channel effects (SCE). Unconventional silicon devices are also researched for extending CMOS scaling beyond the 22nm node.

An increase in current is caused while improving carrier transport and random dopant

Fig 1: MOSFET Structure [1]



fluctuations, due to which un-doped or slightly doped body eliminates threshold voltage variations (Vt). When the size of the transistors is reduced, the source and the gate get so close that it decreases the capability of the gate to influence the potential and the flow distribution of current in the canal area is affected. Thus, adverse consequences, collectively known as "short channel effects" then begin to afflict MOSFET. Pulling down the depth of junction and thickness of gate oxide reduces the short-channel effects. This could be achieved by making the

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depletion depth smaller by increasing doping concentration.

An increase in current is caused while improving carrier transport and random dopant fluctuations, due to which un-doped or slightly doped body eliminates threshold voltage variations (Vt). When the size of the transistors is reduced, the source and the gate get so close that it decreases the capability of the gate to influence the potential and the flow distribution of current in the canal area is affected.

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Scaling of gate oxide can't be done after a level of threshold due to the high tunneling current which is related to smaller gate-oxide thickness. In order to lessen the short-channel effects, other such techniques are also used, one among them being-decreasing the width of the depletion layer lower than the channel to the substrate. A decreased depletion width indicates shrunk depletion area, therefore decreasing the parasitic capacitances. Reducing the depletion width can correspond to reduced gate control over the channel. This results in a slow turning on and off of the channel region.

FinFET offers higher output current per input voltage as compared to MOSFET. Also, it has better speed of switching along with lower power consumption. This is due to the reduced impact of input capacitances. The problem of short channel effect is reduced while using FinFET because of the increased physical separation between the source and the drain regions.

Further Section includes brief description of the technologies and architecture of FinFET. Section 3 shows different inverters using FinFET. Section 4 presents concept of noise margin & results used by researchers. Section 5 includes simulation results using cadence tool followed by section 6 which has conclusion of all the calculations and observations.

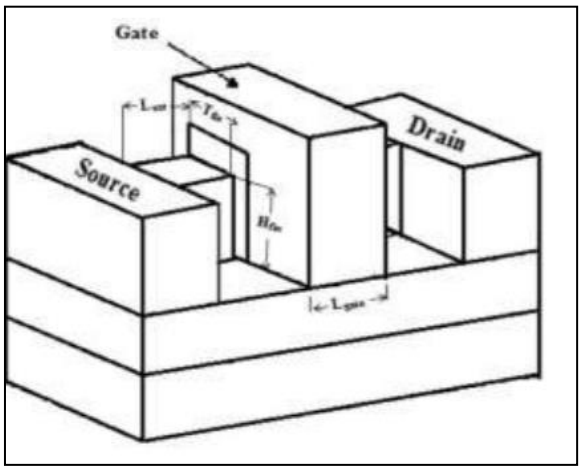
2.0 FinFET Technology

FinFET technology is increasingly being adopted in making of integrated circuits due to many advantages like high level of scalability, lower power consumption, reduced static leakage current and improved operating speed. The FinFET structure is based on Silicon On Insulator (SOI) technology. A fin like structure is formed by the source and the drain on the silicon surface. The gate is wrapped around the channel, which helps in minimizing the leakage current as we have control from three sides of the channel. This structure is called FinFET because it resembles the fins of a fish.

Figure 2 shows the structure of FinFET. It shows the gate covering the channel created between the drain and the source. The channel is then trapped by the gate which gives better control to the device. FinFET having three-dimensional structure offers better performance and saves more power mainly due to low parasitic capacitances and therefore improved on/off characteristics.

It has faster switching speed which is enabled by fully depleted structure. Also, it occupies less wafer area per transistor in order to have a better gain, as the fin height can be changed.

Fig 2: FinFET Structure [2]



3.0 Different Types of FinFET for Inverter

FinFETs have been used in following four modes to give the functionality of the inverter:

1. Shorted Gate (SG) mode: In order to have better control over the channel length both the gates are shorted together.
2. Low Power (LP) mode: Low voltage is applied to the n type FinFET and high voltage to the p type FinFET. It is to vary the threshold voltage.
3. Independent Gate (IGn) mode: In this type, p type is shorted to its gate and n type FinFET is given low voltage.

4. Independent Gate (IGp) mode: In this type, n type is shorted to its gate and p type FinFET is given high voltage.

Figure 3 shows the different types of FinFET inverters.

4.0 Noise Margin

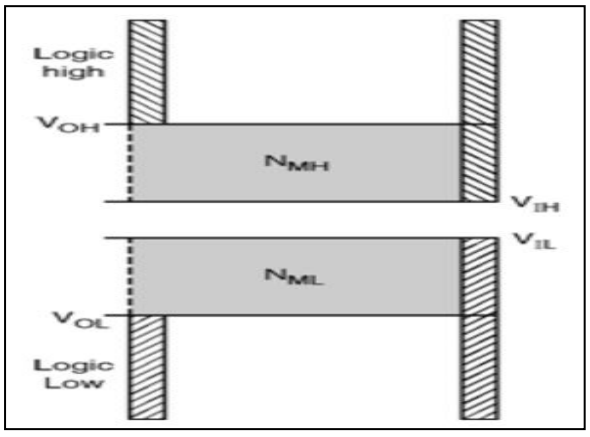
Noise margin was originally described as "the maximum allowable spurious signal that can be accepted by a device when used in a system while still giving correct operation".

Noise margin is the maximum difference between the expected and the actual output, provided the operation of the circuit is not affected.

Ideally, if voltage at the input is given logic '0', then the voltage at the output terminal is expected to come out to be logic '1'. Therefore, in other words, V $input_{low}$ (V_{IL}) is '0'V & V $output_{high}$ (V_{OH}) is 'Vdd'V. Similarly, if input is at logic '1', then voltage at output is expected to be logic '0'. Therefore, it can be termed as, if V $input_{high}$ (V_{IH}) is 'Vdd', then V $output_{low}$ (V_{OL}) is '0'V.

Figure 4 shows the Noise Margin High (NM_H) and Noise Margin Low (NM_L). Figure 5 shows the calculation of Noise Margins from nearly ideal Voltage Transfer Characteristics (VTC) of an inverter.

Fig. 3: Noise Margin Low & Noise Margin High



Noise Margins for nearly ideal VTC can be seen as:

Noise Margin $_{Low}$ (NM_L) = $V_{IL} - V_{OL}$ => 0 – 0 = 0

Noise Margin $_{High}$ (NM_H) = $V_{OH} - V_{IH}$ => $V_{dd} - V_{dd}$ = 0

Fig. 4: Types of FINFET Inverters [3]

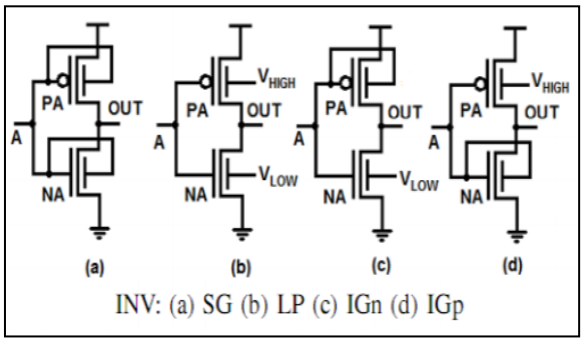


Fig 5: Calculation of NM Using Values from Graph

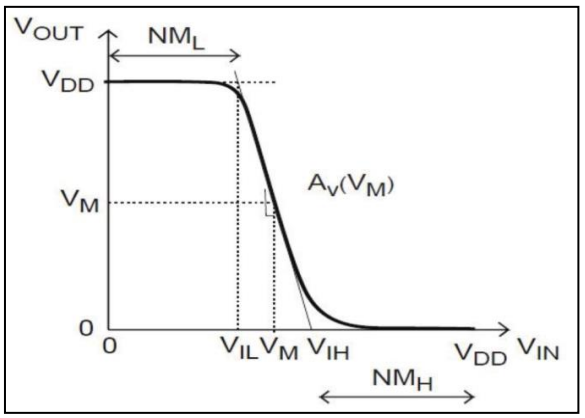
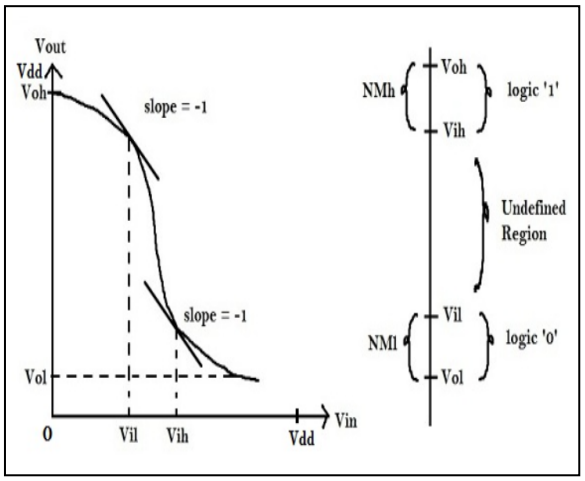


Figure 6 shows the VTC and Noise margins of any practical inverter, where, V_{il} and V_{ol} do not coincide and similarly V_{oh} and V_{ih} do not coincide.

Fig 6: VTC and Noise Margins of a Practical Inverter



Hence, if the input voltage (V_{in}) is somewhere in the middle of V_{ol} ($V_{\text{output low}}$) and V_{il} ($V_{\text{input low}}$), it will be identified as logic - 0, and outcome is an acceptable output. Likewise, if input voltage (V_{in}) is in the range of V_{ih} ($V_{\text{input high}}$) & V_{oh} ($V_{\text{output high}}$), it will then be identified as logic-1 and will again result into allowed output. If the input voltage is in the range between V_{ih} and V_{il}, then the logic is undefined (as shown in Fig. 6), its neither logic 0 nor logic 1.

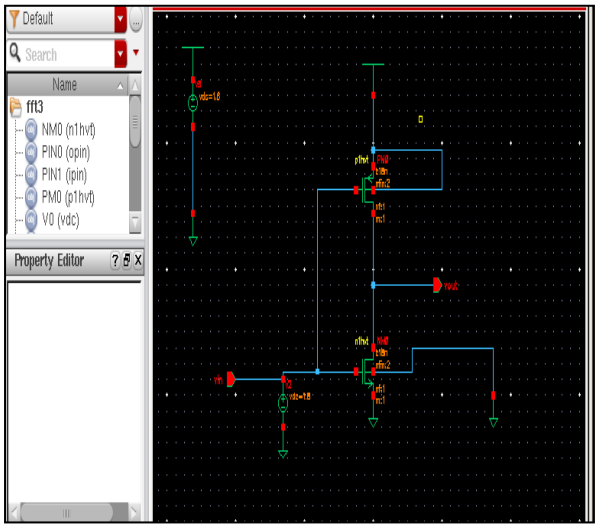
5.0 Results

The schematics of four types of inverters namely independent gaten mode, independent gatep mode, shorted gate mode and low power mode (as discussed in section 3), were drawn in Cadence Virtuoso and DC analysis was done in each case to draw the voltage transfer characteristics. For all these modes, voltages are observed manually from the graphs using pointer in virtuoso. These voltage values (V_{il} , V_{oh} , V_{ih} , V_{ol}) were then used to get noise margin values through the formula shown in section 4. Table 1 shows the parameter values used in simulations.

Table 1: Parameters Used in Simulations (Approximate Values)

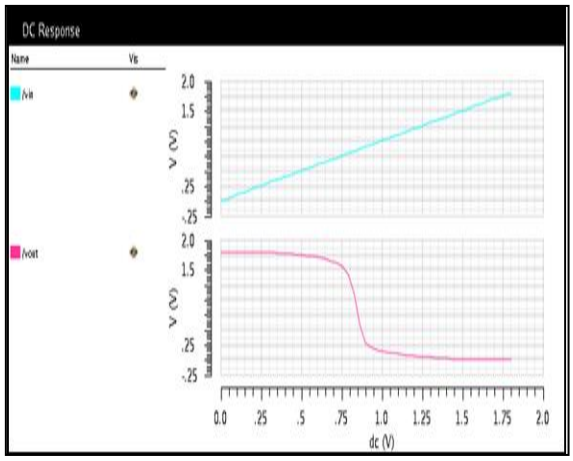
Gate length	18nm
Vg	0-1.8
Vdd	1.8
Vhigh	1.8
Vlow	Gnd

Fig. 7: Schematic of IGn Mode



Figures 7 to figure 14 show the screenshots of the schematics and the output graphs of DC analysis of inverters

Fig 8: DC response graph (VTC) of IGn mode



5.1 Independent gate (IGp) mode

Fig 9: Schematic of IGp Mode

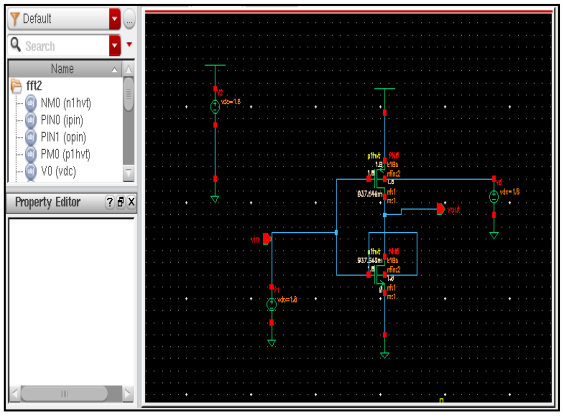
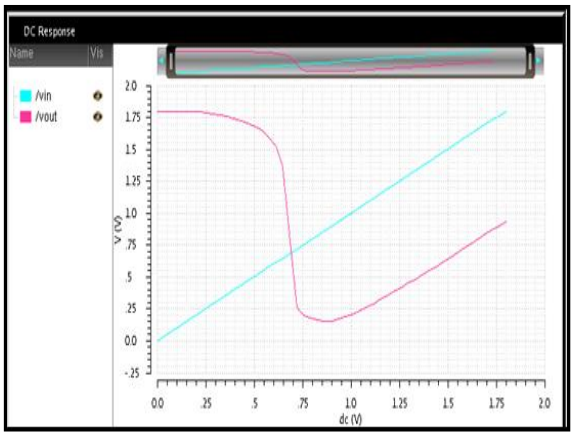


Fig 10: DC Response Graph (VTC) of IGp Mode



5.2 Shorted gate mode

Fig 11: Schematic of Shorted Gate Mode

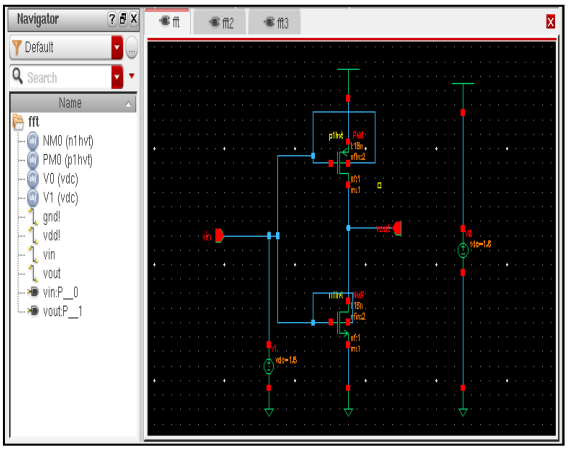
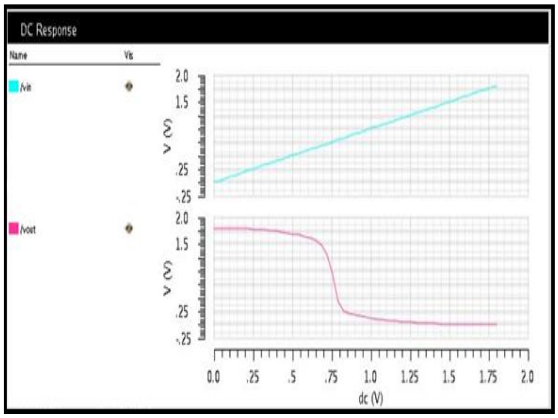


Fig 12: DC Response Graph (VTC) of Shorted Gate Mode



5.3 Low power mode

Fig 13: Schematic of Low Power Mode

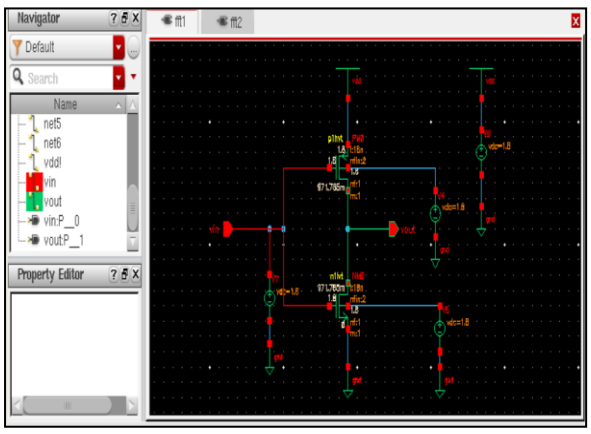
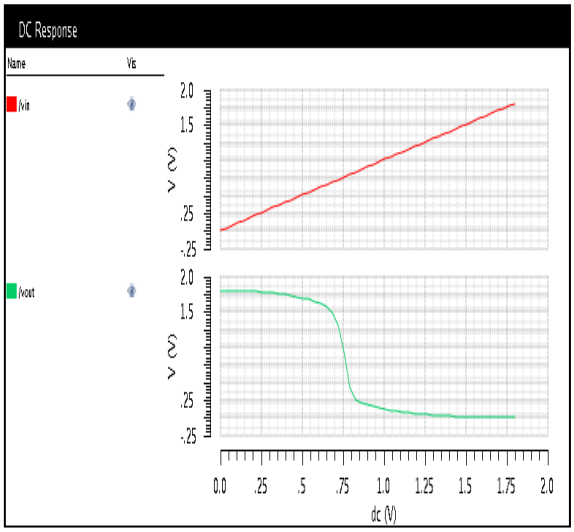


Fig 14: DC Response Graph (VTC) of Low Power Mode



5.4 Noise Margins Calculation

Table 2 shows the V_{ih}, V_{oh}, V_{il}, V_{ol}, NM_L and NM_H values of all 4 types of FinFET Inverters

Table 2: V_{ih}, V_{oh}, V_{il}, V_{ol}, NM_L and NM_H Values

Type	VIH	VOH	VIL	VOL	NML = VIL-VOL	NMH = VIH-VOH
SG	1.38	1.12	0.75	0.65	0.1	0.26
LP	1.6	0.823	0.5	0.16	0.34	0.77
IGp	1.21	1.14	0.61	0.49	0.12	0.07
IGn	1.16	1.09	0.66	0.54	0.12	0.07

6.0 Conclusions

Noise margin low is when the input voltage supplied is low. For noise margin low, it is observed that the low power mode has the highest noise margin followed by the independent gate mode of p-type and n-type both with a noise margin almost equal to each other. Lowest noise margin is for shorted gate mode.

Noise margin high is the one if the voltage applied is high, and for this mode also low power mode has the highest noise margin followed by shorted gate mode and then least noise margins for the independent gate modes.

Thus, Low power mode of FinFET inverter is better than the rest of the FinFET inverters, as far as noise margin parameter is concerned.

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