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Single OTRA based Low Voltage Square Root Circuit

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ABSTRACT

This paper presents an analog square root circuit using single Operational Transresistance Amplifier (OTRA). It can be used to obtain the square root of the low input voltage. This circuit does not use any external passive component and hence is suitable for integration. The proposed circuit is verified with the help of simulations using 0.18µm CMOS parameters on PSPICE. The theoretical observations are in accordance with the simulation result.

Keywords: *Analog Square Root Circuit; OTRA; Low Voltage.*

1.0 Introduction

Analog square root circuit is used extensively in measurement [1], low voltage analog multiplier [2] and operational trans-conductance-amplifier [3]. Many circuits have been proposed for implementation of square root circuit [4-5].

This square root circuit has been implemented using operational tranresistance amplifier. OTRA has gained immense popularity in recent times.

It is used as an alternate active block for implementation of analog circuits [6-7] since it inherits all the advantages of current mode techniques.

It is a three-terminal current input voltage output device. The input is free from parasitic capacitances and resistances since the input terminals are virtually grounded internally.

OTRA has been implemented using CMOS in various forms in the literature [7]. This paper presents a low voltage analog square root circuit which is suitable for integration.

1.2 Proposed square root circuit

1.3 OTRA

OTRA is a Current Controlled Voltage Amplifier and its V-I relationship can be defined by the following matrix where R_m is the transresistance gain of OTRA.Ideally R_m is infinite which forces input currents to be equal. Hence negative feedback is employed in OTRA. The CMOS based implementation of OTRA is shown in Fig. 1 and its circuit symbol is depicted in Fig. 2.

$$\begin{bmatrix} V_P \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_P \\ I_n \\ I_o \end{bmatrix} \quad \ldots (1)$$

Fig 1: OTRA Schematic [8]

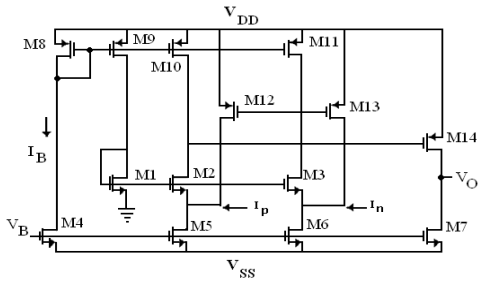

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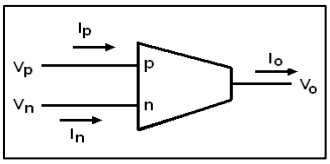
Fig 2: OTRA Schematic Symbol



2.0 Square root circuit

Square root structure based on OTRA is shown in Fig. 3. The MOSFET M_1operates in saturation region whereas M_2, and M_3operatein triode region. In triode region, the drain current through MOS transistor is given by:

$$I_D = K\frac{W}{L}\left((V_{GS} - V_T) - \frac{V_{DS}}{2}\right)V_{DS} \quad \ldots (2)$$

And the drain current in saturation region is given by:

$$I_D = \frac{K}{2}\frac{W}{L}(V_{GS} - V_T)^2 \quad \ldots (3)$$

where *K* ,*W* and *L* respectively represent the transconductance,the width and the length of the MOSFETchannel.

Using (2) and (3) the currents through inverting (I_n) and non-inverting (I_p) terminal of the OTRA can respectively be given as

$$I_n = K\left(\frac{W}{L}\right)_{2,3}((V_b - V_T)V_i - \frac{1}{2}{V_i}^2) + \frac{K}{2}\left(\frac{W}{L}\right)_1((V_o + V_1) - V_T)^2 \quad \ldots (4)$$

$$I_p = K\left(\frac{W}{L}\right)_{2,3}((V_a - V_T)V_i - \frac{1}{2}{V_i}^2) \quad \ldots (5)$$

As R_m approaches infinity, current through inverting (I_n) and non-inverting (I_p) terminal of the OTRA tendto be equal. Thus, equating (4) and (5) results in

$$K\left(\frac{W}{L}\right)_{2,3}\left((V_a - V_T)V_i - \frac{1}{2}{V_i}^2\right) = K\left(\frac{W}{L}\right)_{2,3}((V_b - V_T)V_i - \frac{1}{2}{V_i}^2) + \frac{K}{2}\left(\frac{W}{L}\right)_1((V_o + V_1) - V_T)^2 \quad \ldots (6)$$

If V_1 is chosen such that $V_1 = V_T$

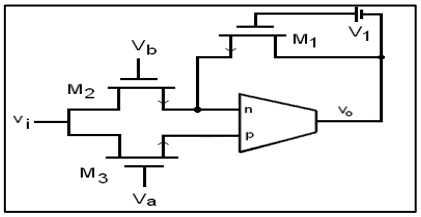
$$V_O = \sqrt{\frac{2V_i\left(\frac{W}{L}\right)_{2,3}(V_a - V_b)}{\left(\frac{W}{L}\right)_1}}$$

$$V_o = A\sqrt{V_i}$$

Where$A = \sqrt{\frac{2\left(\frac{W}{L}\right)_{2,3}(V_a - V_b)}{\left(\frac{W}{L}\right)_1}}$

The proposed square root circuit does not use any passive component and hence consumes less chip area. Therefore, this circuit is also suitable for integration.

Fig 3: Square Root Circuit Using MOS Transistors



3.0 Simulation Results

The proposed circuit for square root is verified through PSPICE simulation program using 0.18 µm CMOS process parameters. The dual supply voltage for OTRA is 1.5V. The MOS transistors aspect ratios used in OTRA are given in Table 1. The transistors M_2 and M_3 have aspect ratio of 5 (W/L = 5µm/1µm). Transistor M1 has aspect ratio of 1 (W/L = 1µm/1µm). Voltages Va, V_b and V_1 are chosen to be 1.05V, 1V and 0.4V respectively.

Table I: MOS Transistors Aspect Ratios for OTRA

Transistor	W(µm)/L(µM)
M_{01}-M_{03}	100/2.5
M_{04} , M_{07}	10/2.5
M_{05} , M_{06}	30/2.5
M_{08} - M_{011}	50/2.5
M_{012} ,M_{013}	100/2.5
M_{014}	50/2.5

3.1 Dc characteristics

The DC Characteristics of the proposed analog Square root circuit are analyzed. The input Voltage Vi is swept from 0mV to 500mV in steps of 1mV. The curve between output (Vo) and input (Vi) voltages is plotted and is shown in Fig. 4. It is observed that the output voltage closely follows the square root of input voltage.

Fig 4: Simulation Result - V_0 vs V_{in}

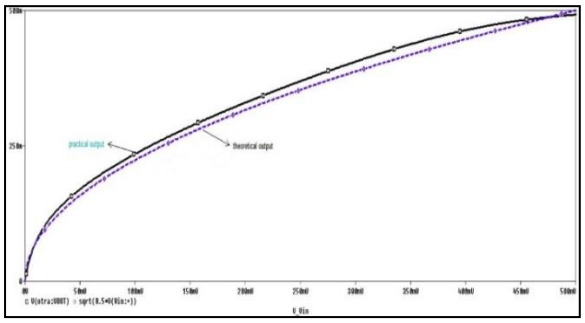


Fig 5: Transient Response

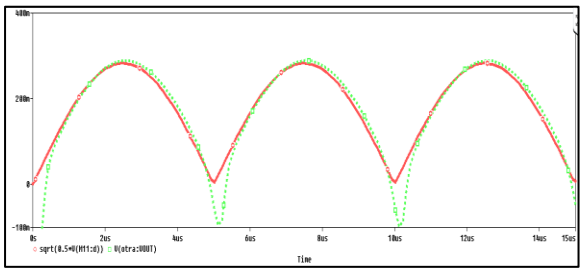
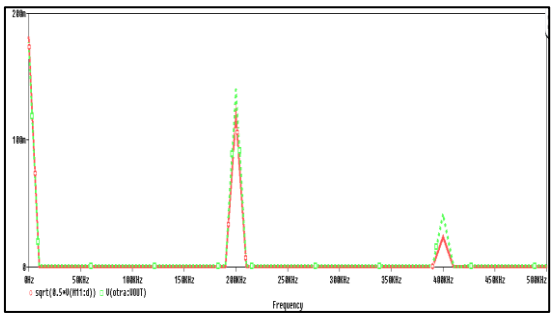


Fig 6: Frequency Spectrum



3.2.Transient characteristics

The Transient Characteristics of the proposed analog Square root circuit are analyzed.A squared sinusoidal voltage of frequency 100kHz and amplitude 400mV is given as input. The output voltage (Vo) as well as expected output is plotted with respect to time and is shown in Fig. 5.The Frequency Spectrum of the proposed circuit is also analysed from 0Hz to 500KHz and is shown in fig 6.

The practical result matches the theoretical result.

4.0 Conclusions

A Low Voltage Analog Square Root circuit is proposed and verified using PSPICE. The circuit is made without using any passive elements and hence can be easily fabricated.The proposed circuit works for all input voltages less than 500mV. The Square Root circuit can be used in measurements and instrumentation and for various other purposes. With the added benefits of OTRA as stated previously, this structure overcomes the limitations of Voltage mode circuits like OPAMP.

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