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Comparative Study of CMOS Logic and Modified GDI Technique for Basic Logic Gates and Code Convertor

Arjun Sehrawat, Vandana Khanna** and Kushal Jindal****

ABSTRACT

For designing low power digital circuits with better reliability and performance along with less propagation delay, Gate Diffusion Input (GDI) is one such technique. It also significantly reduces the area and delay of a circuit. It is a low power technique which requires a smaller number of transistors to achieve desired outputs with lower design complexity as compared to CMOS logic or Pass Transistor Logic. In a basic GDI cell, 3 terminals namely Gate, Source and Drain are treated as inputs. In this work, circuits like logic gates, and Binary to Gray code convertor have been designed using CMOS logic and a Modified GDI technique. Also, the power dissipation of all these circuits have been calculated and compared for CMOS and Modified GDI. The designing and simulations have been done on Cadence Virtuoso tool in 90 nm technology and power supply voltage has been taken as 1 V.

Keywords: *CMOS Logic; GDI Technique; MGDI; Code Convertor.*

1.0 Introduction

Nowadays, as the design complexities on IC chips are increasing exponentially. There is an urge to develop and examine such power reducing techniques which could provide low power consumption, less complex design, high speed performance and high reliability without compromising any functionality of a circuit design. Currently, the most popular technology used to design circuits is CMOS technology, but it dissipates a lot of power during transistor switching and also leakage current flow when not in switching activity. Some other techniques which were introduced afterwards were Pass Transistor Logic (PTL), Complementary PTL, Gate Diffusion Input (GDI) etc. As compared to static CMOS logic, PTL had high speed due to low node capacitances, lesser number of transistors resulting in low power dissipation and lower design complexity. The main disadvantage of PTL was logic degradation in the long chain of pass transistors.

GDI was introduced as a promising approach for low power dissipation, less design complexity, less chip area and high performance. Basic GDI Cell consists of only two transistors which can implement various complex logic functions. The disadvantage of GDI technique is that it does not give the complete output swing of a desired output state. In this paper, we have examined the Modified GDI technique for designing and simulations of multiple logic functions and then compare it with the existing CMOS logic in terms of transistors used and total power dissipation. The Modified Gate Diffusion Input (MGDI) functioning and diagram is represented in Section 2. Implementation of logic functions using CMOS and MGDI has been discussed in Section 3, and the design and implementation of binary to gray code converter is described in Section 4. The results and the comparative analysis has been carried out in Section 5. The work is concluded in Section 6.

2.0 Modified Gate Diffusion Input

MGDI is a low-power design technique and is an upgraded form of GDI technique. Unlike the basic GDI cell where the substrate connections of NMOS and PMOS are connected to sources of the respective gates; in Modified GDI technique, the Gate terminal, and the Source of PMOS and NMOS are connected to the input signals and substrates of NMOS and PMOS are connected to ground and VDD respectively as shown in Fig. 1 [1].

**Corresponding author; Department of EECE, The NorthCap University, Gurugram, Haryana, India (E-mail: vandanakhanna@ncuindia.edu)*

, Department of EECE, The NorthCap University, Gurugram, Haryana, India*

Fig. 1 (a): Basic GDI Cell

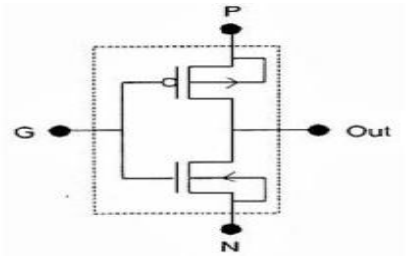
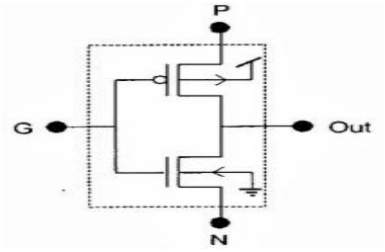


Fig. 1 (b): Modified GDI Cell [1]



In the Fig 1, the cells consist of 3 inputs: G, P, and N where G is the Gate terminal, P and N are the Source terminals of PMOS and NMOS. The substrates of PMOS and NMOS are connected to the source terminals in the basic GDI cell and are connected to VDD and Ground respectively in the MGDI cell. The Drain terminals of PMOS and NMOS are connected to retrieve the desired output.

This exceptional arrangement of Modified GDI cell provides considerable reduction of both sub-threshold leakage and gate leakage. MGDI approach is quite suitable for design of low power and high-speed logic circuits as it requires lesser number of transistors. At the same time, this approach improves static power dissipation and the logic swing and allows easy top-down design by using a small cell library.

Table 1 shows the implementation of some basic logic functions which can be implemented using two transistors only by MGDI Technique [2]. Universal logic gates NAND ((A.B)') and NOR ((A+B)') requires 4 transistors using MGDI Technique which is same number as required in CMOS Technology.

Following are the limitations of the GDI cell:

- When the PMOS transmits logic 0 it passes degraded output.
- When the NMOS transmits logic 1 it passes degraded output.

However, the full output swing is seen in the transient analysis when PMOS transmits logic 1 and NMOS transmits logic 0 [3].

Table 1: Generation of Logic Functions from a Modified GDI Cell

N	P	G	Output	Function
0	1	A	A	Inverter
0	B	A	A' B	F1
B	1	A	A'+ B	F2
1	B	A	A + B	OR
B	0	A	A. B	AND
C	B	A	A' B+AC	MUX

3.0 Design of Logic Gates using CMOS Logic and Modified GDI Techniques

Schematics for logic gates such as OR Gate, AND Gate, NOR Gate and NAND Gate are designed in both CMOS and MGDI techniques to determine the number of transistors used and comparing its total power dissipation.

Table 2: Binary to Gray Converter Truth Table

BINARY INPUT				GRAY CODE OUTPUT			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Figures 2-5 show the schematics of all logic gates designed using CMOS logic and Modified GDI techniques. Transient analysis is done for all these schematics and there were no significant changes in waveforms generated when compared with each other for each logic gate.

3.1 Binary to gray code converter

Gray code is a non-weighted system which means it does not depend on positional value of digit. It is also called cyclic code or reflective code because it requires only one bit change in every transition from one value to the next value. An interesting application for Exclusive-OR gate (XOR) is a logic circuit to change a binary number to its equivalent in gray code and vice versa. XOR gates are used in cascaded form to build this type of code converter [4]. Table 2 represents the truth table for 4-bit binary to gray code converter. This code converter requires 3 XOR gates, the circuit diagram of binary to gray code converter is shown in Fig. 6. Here, in3 in2 in1 in0 represent the four bit binary input, and out3 out2 out1 out0 represent the 4-bit Gray code; out3 would be same as in3, so it is not shown in the circuit diagram.

Fig. 2(a): NAND Gate Using CMOS

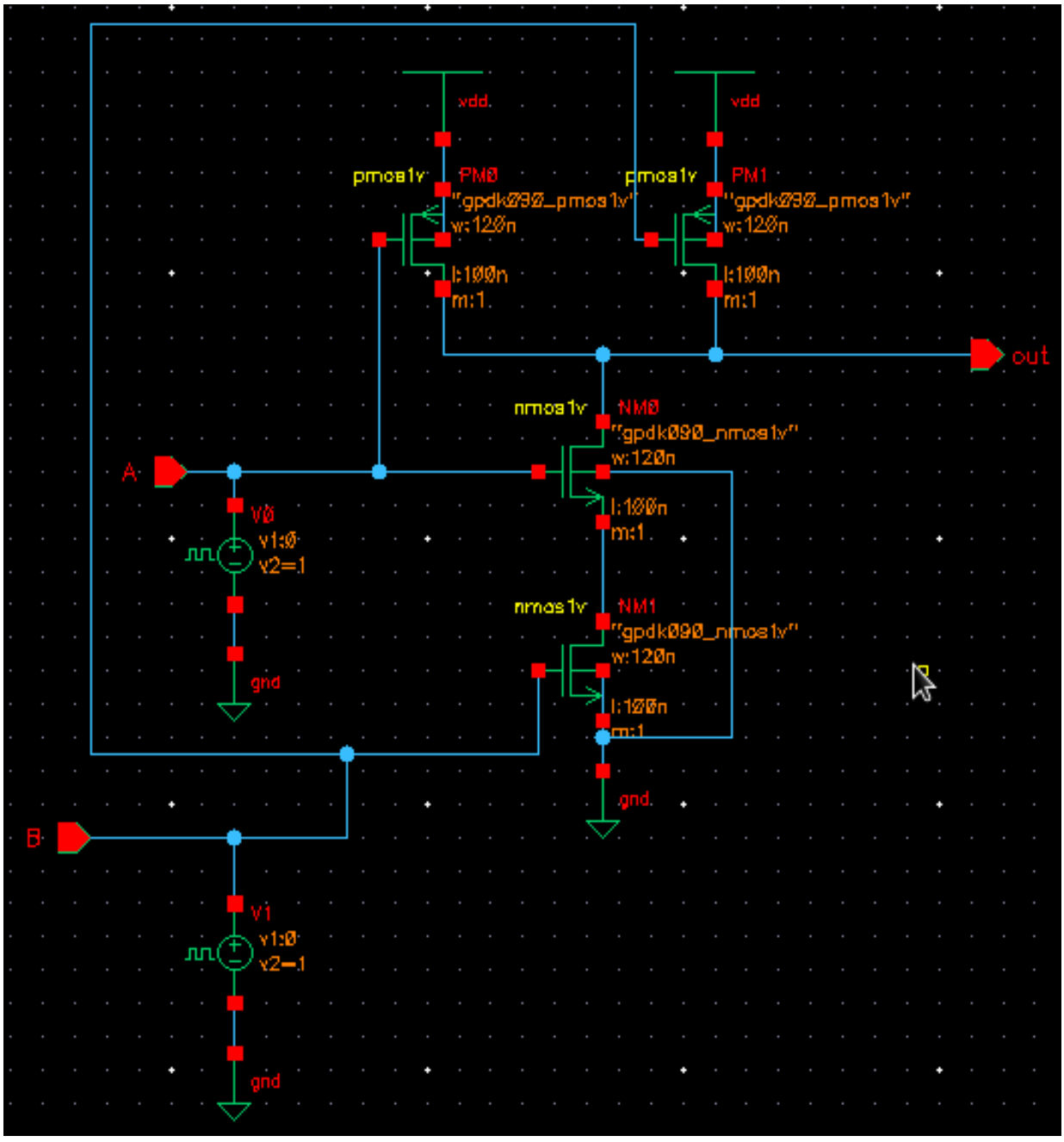


Fig. 2(b): NAND Gate Using MGDI

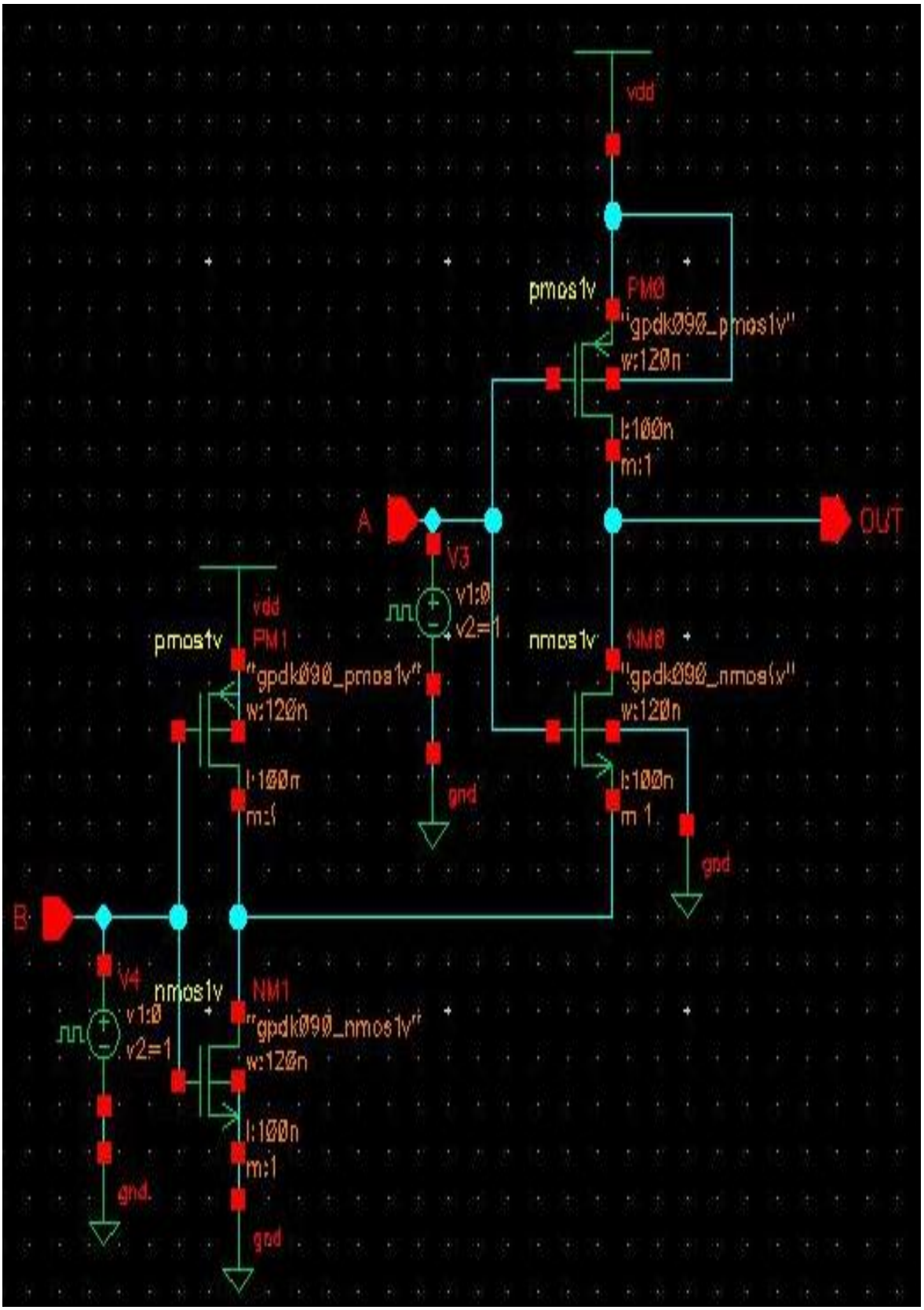


Fig. 3(a): NOR Gate using CMOS

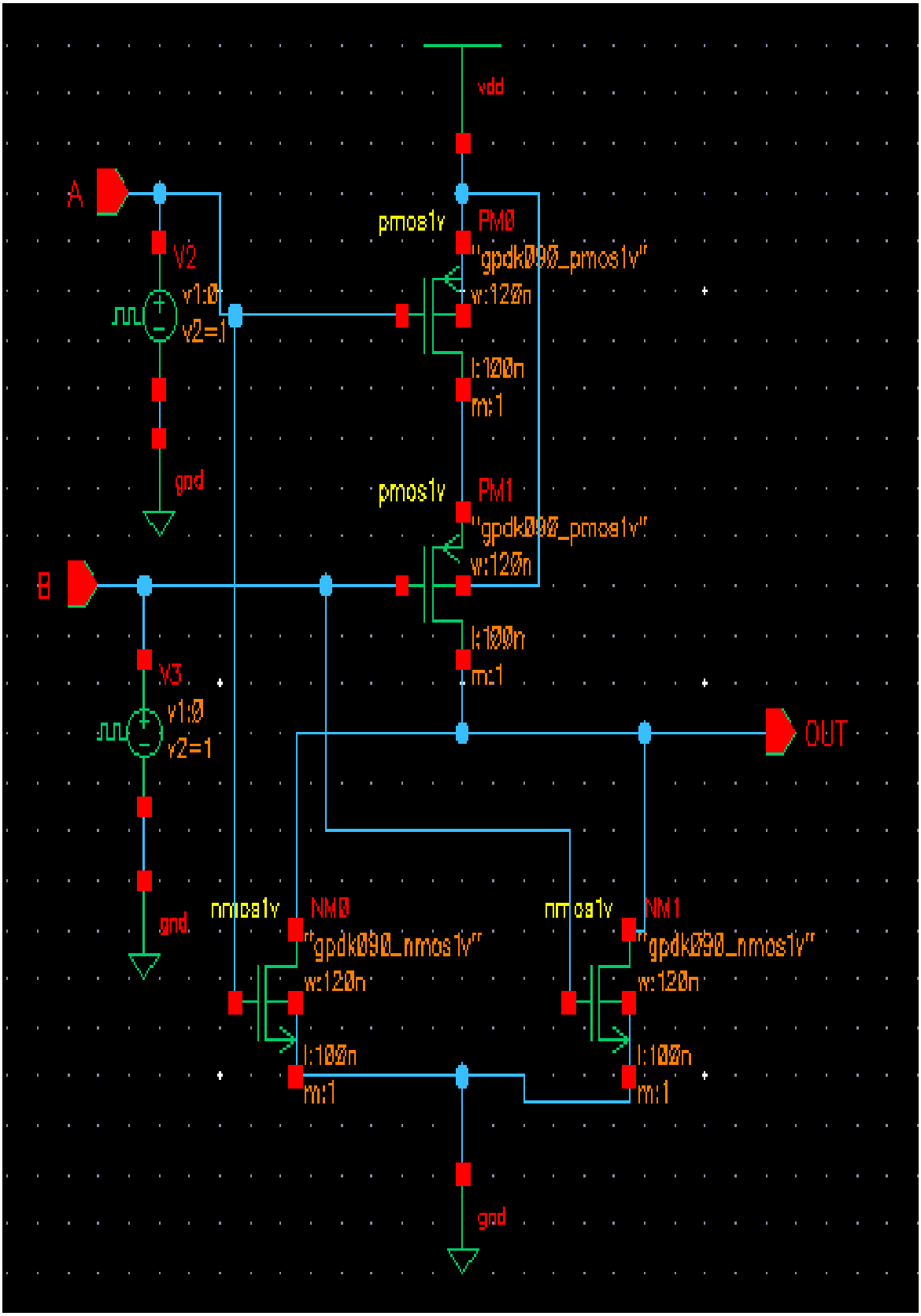


Fig. 3(b): NOR Gate Using MGDI

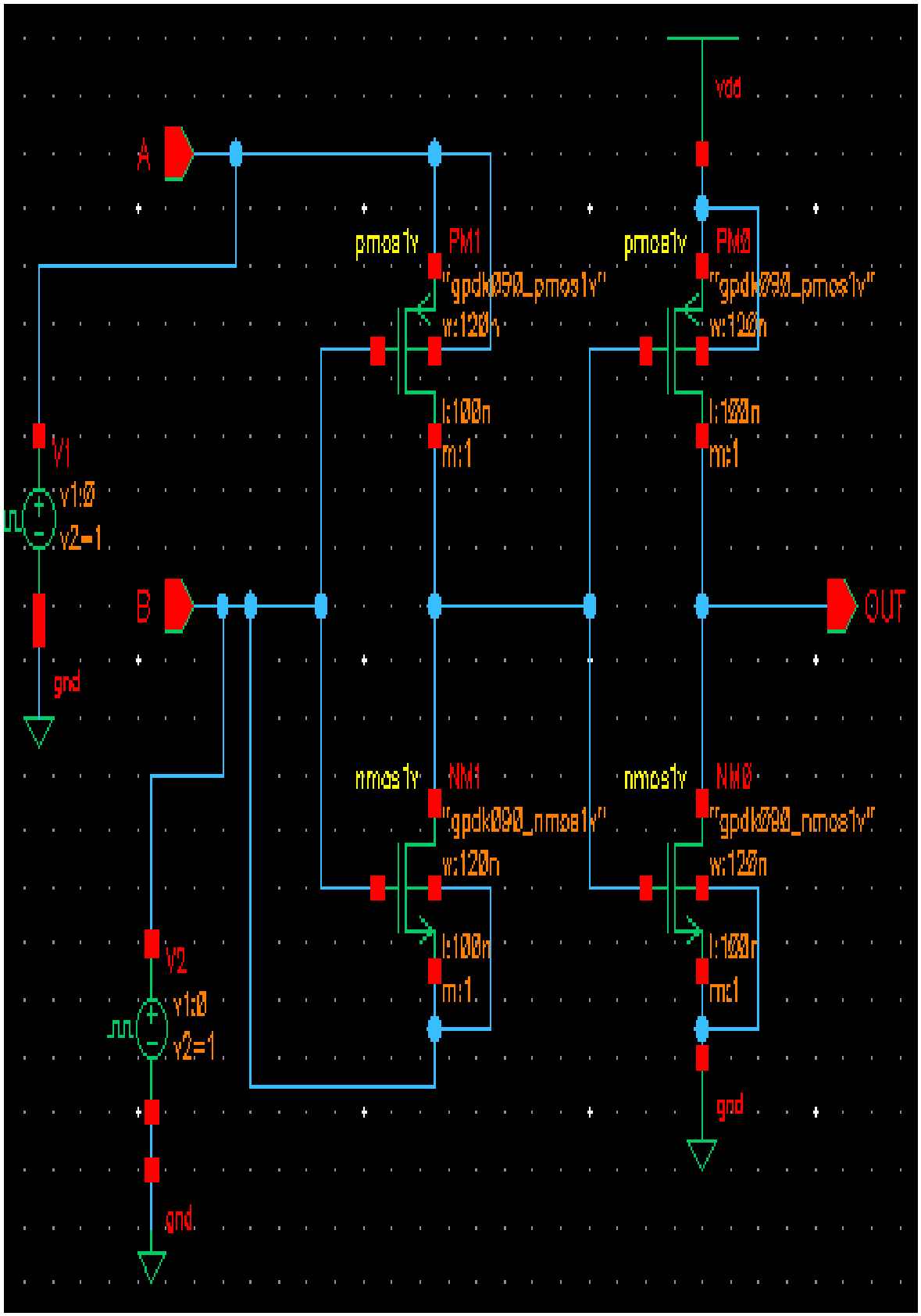


Fig. 4(a): AND Gate Using CMOS

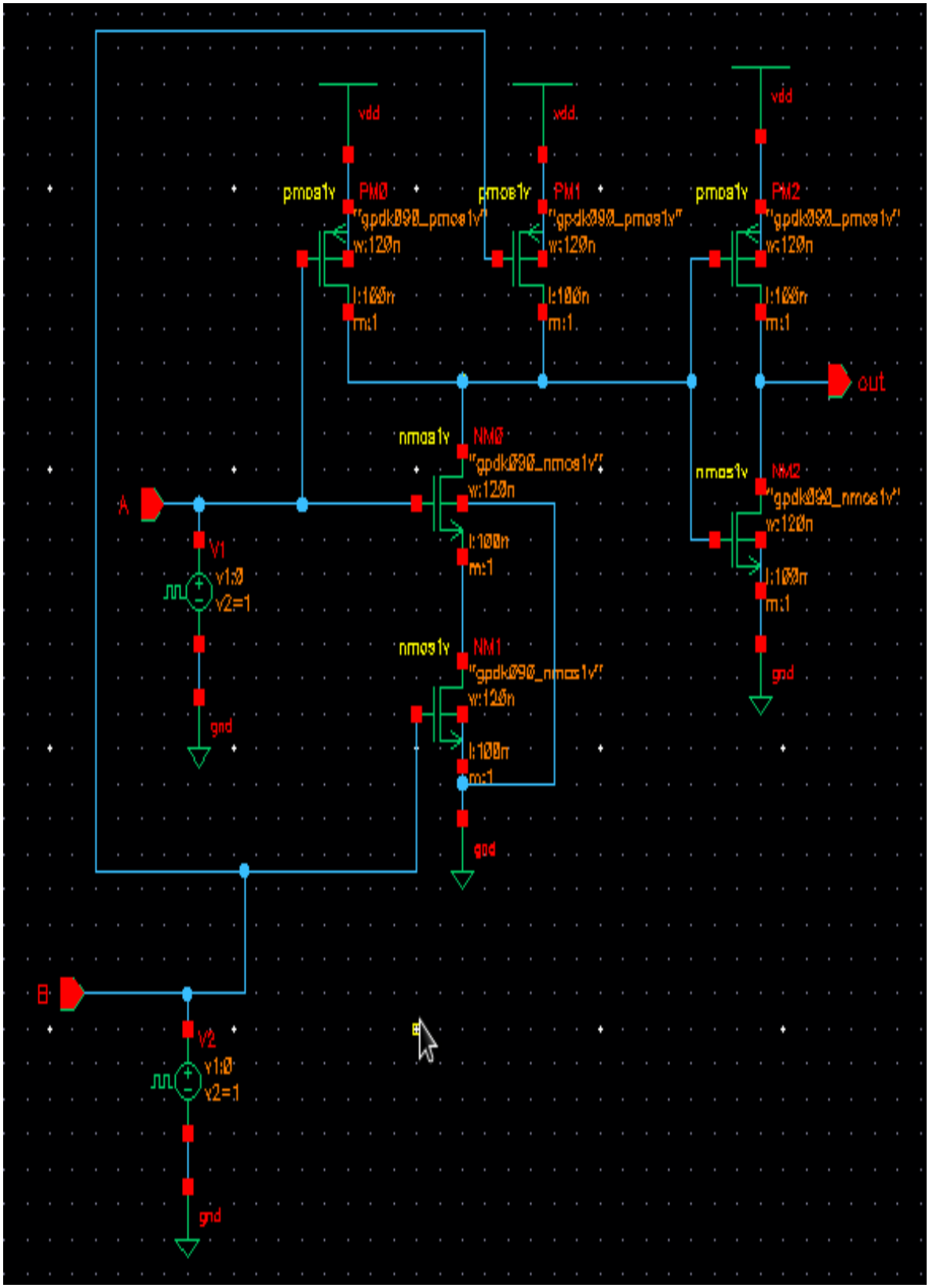


Fig. 4(b): AND Gate Using MGDI

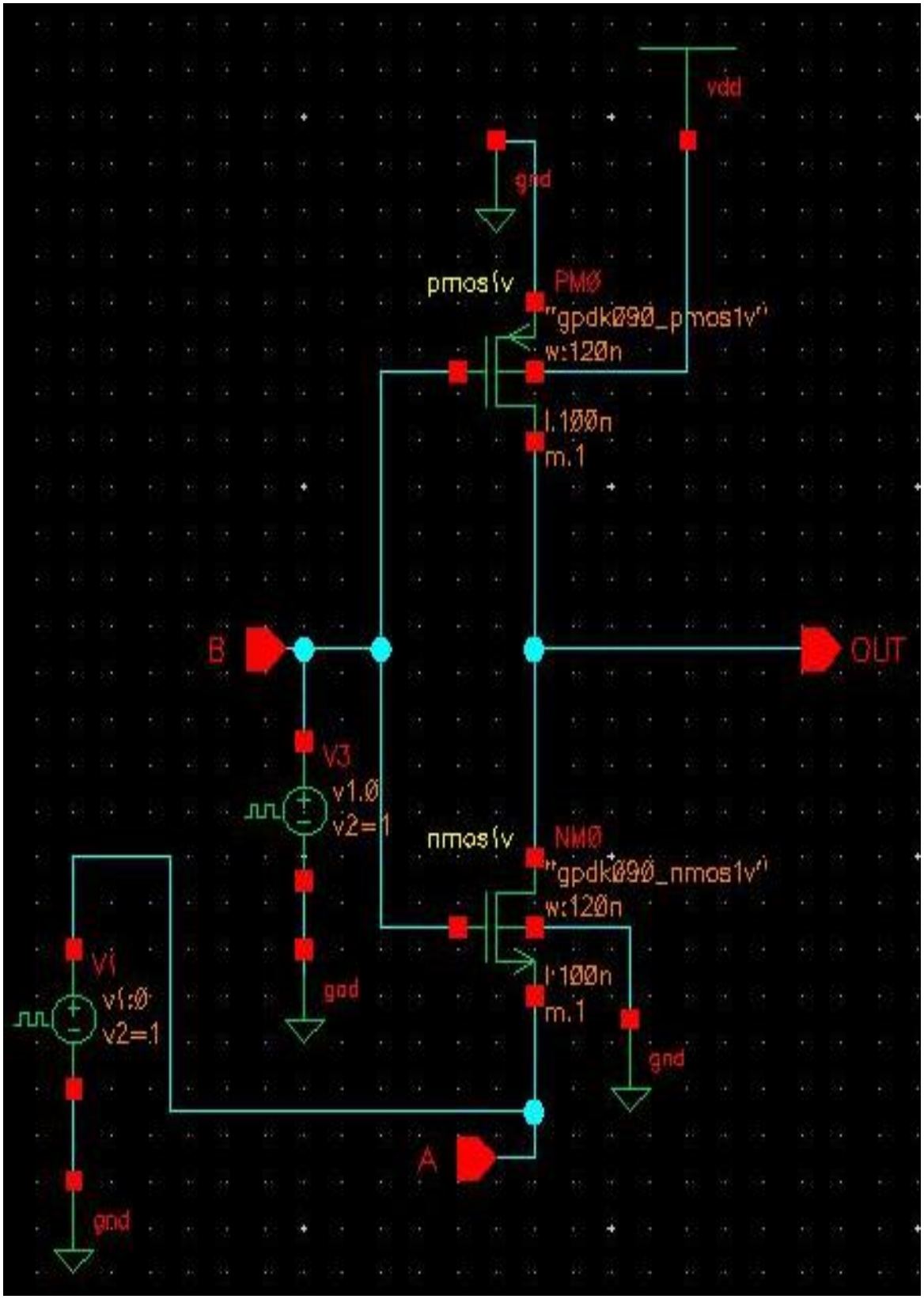


Fig. 5(a): OR Gate Using CMOS

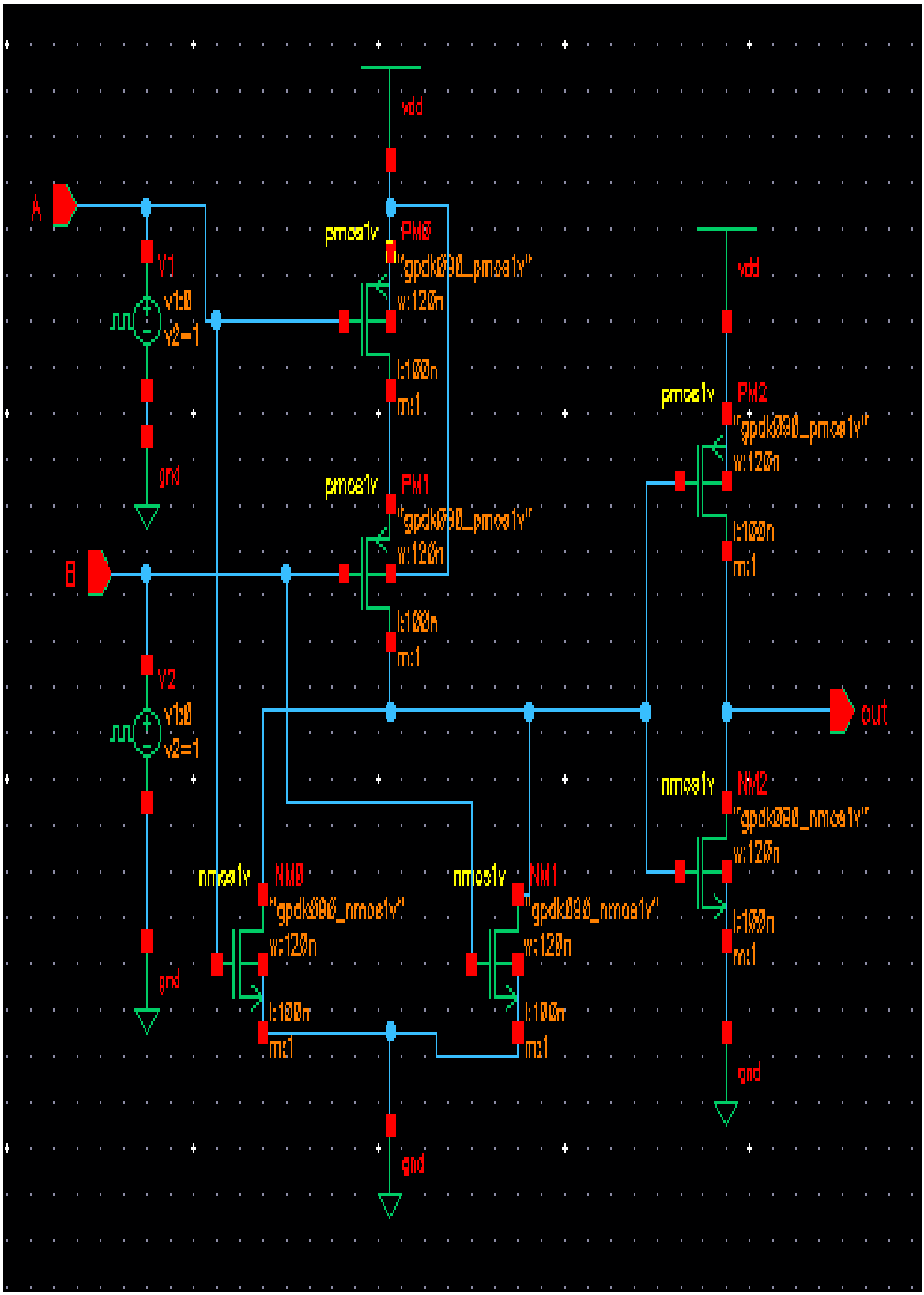


Fig. 5(b): OR Gate Using MGDI

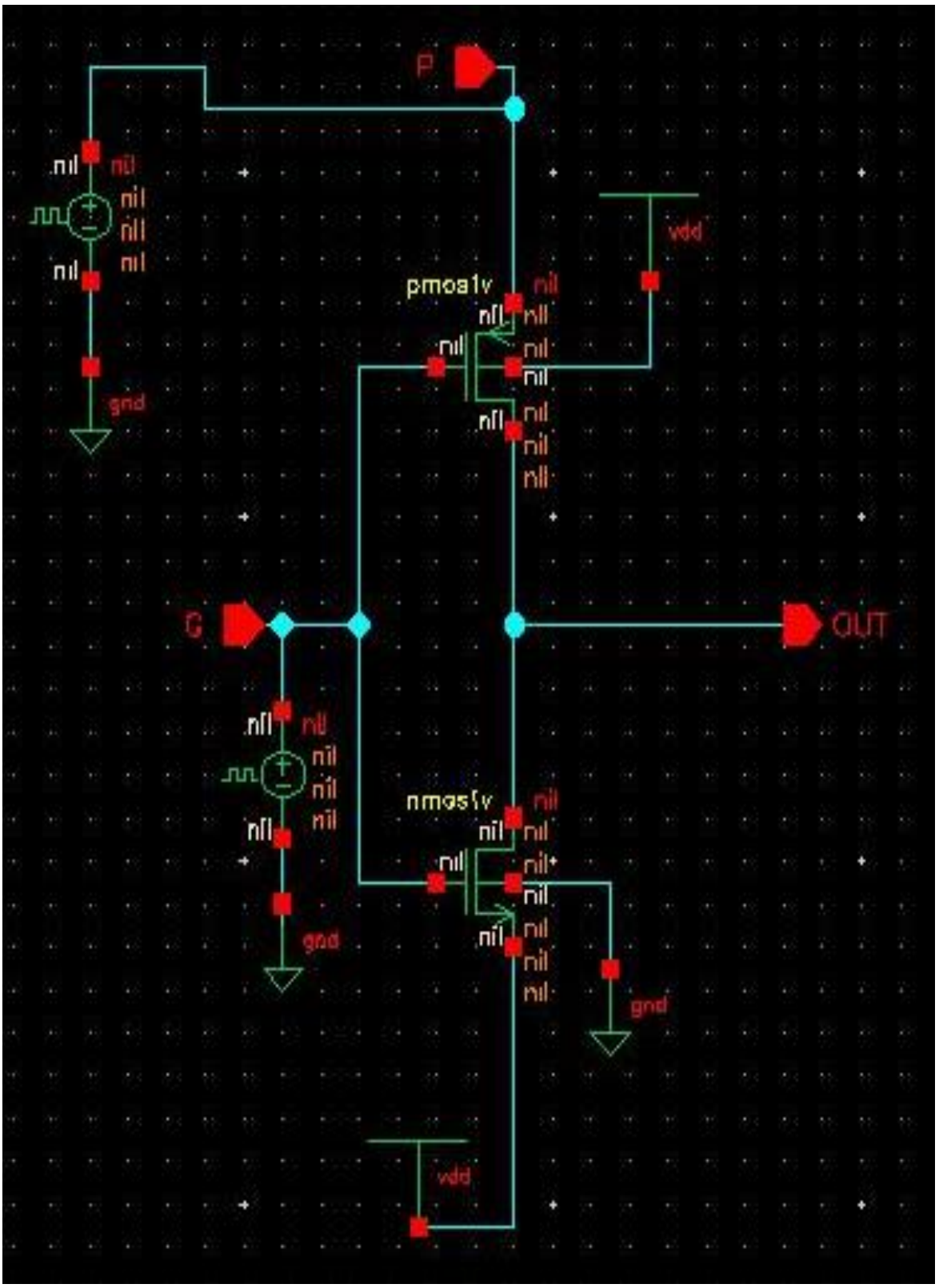


Fig. 6: Binary to Gray Code Converter

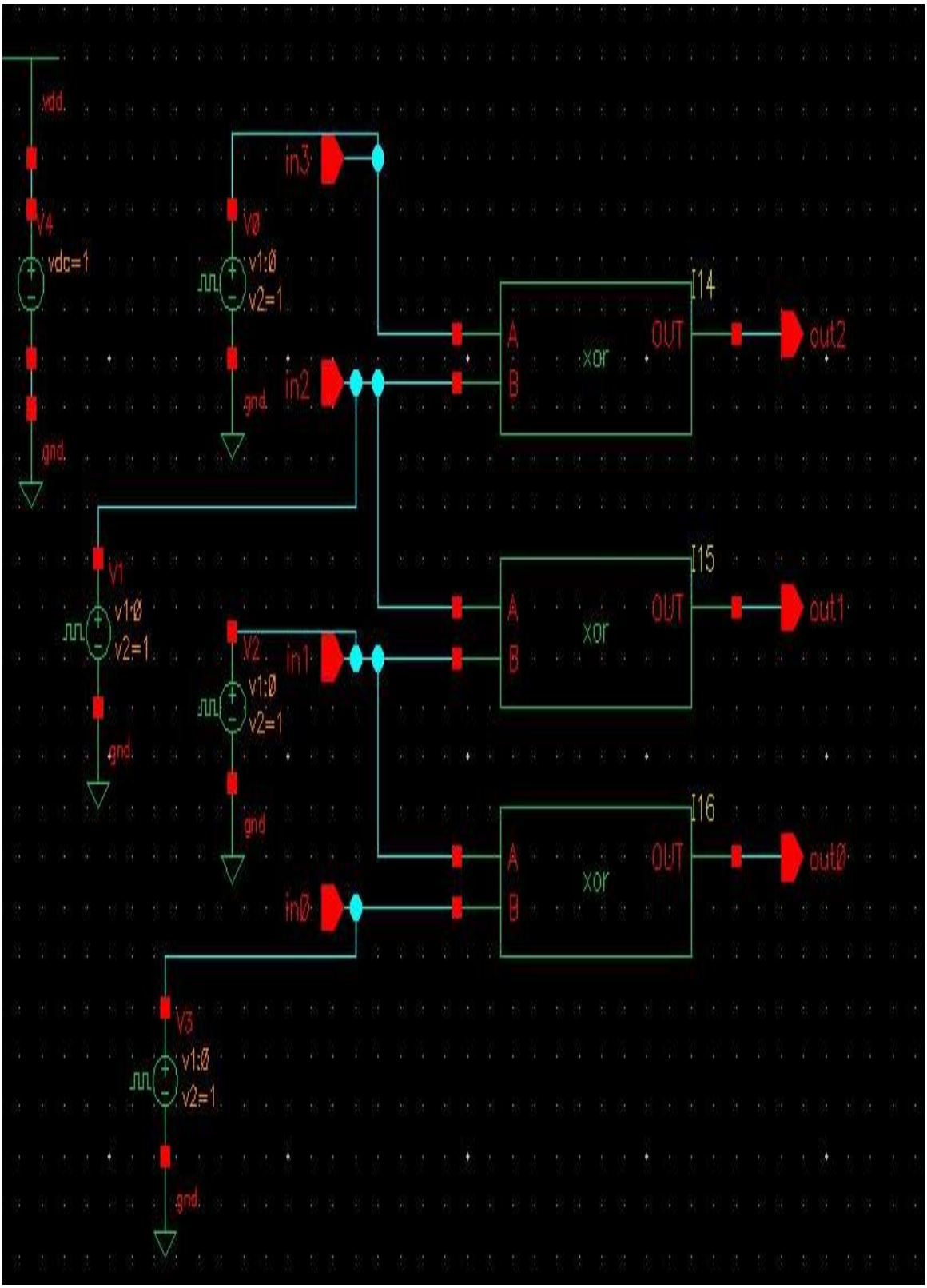


Fig. 7: XOR Gate Using CMOS Logic

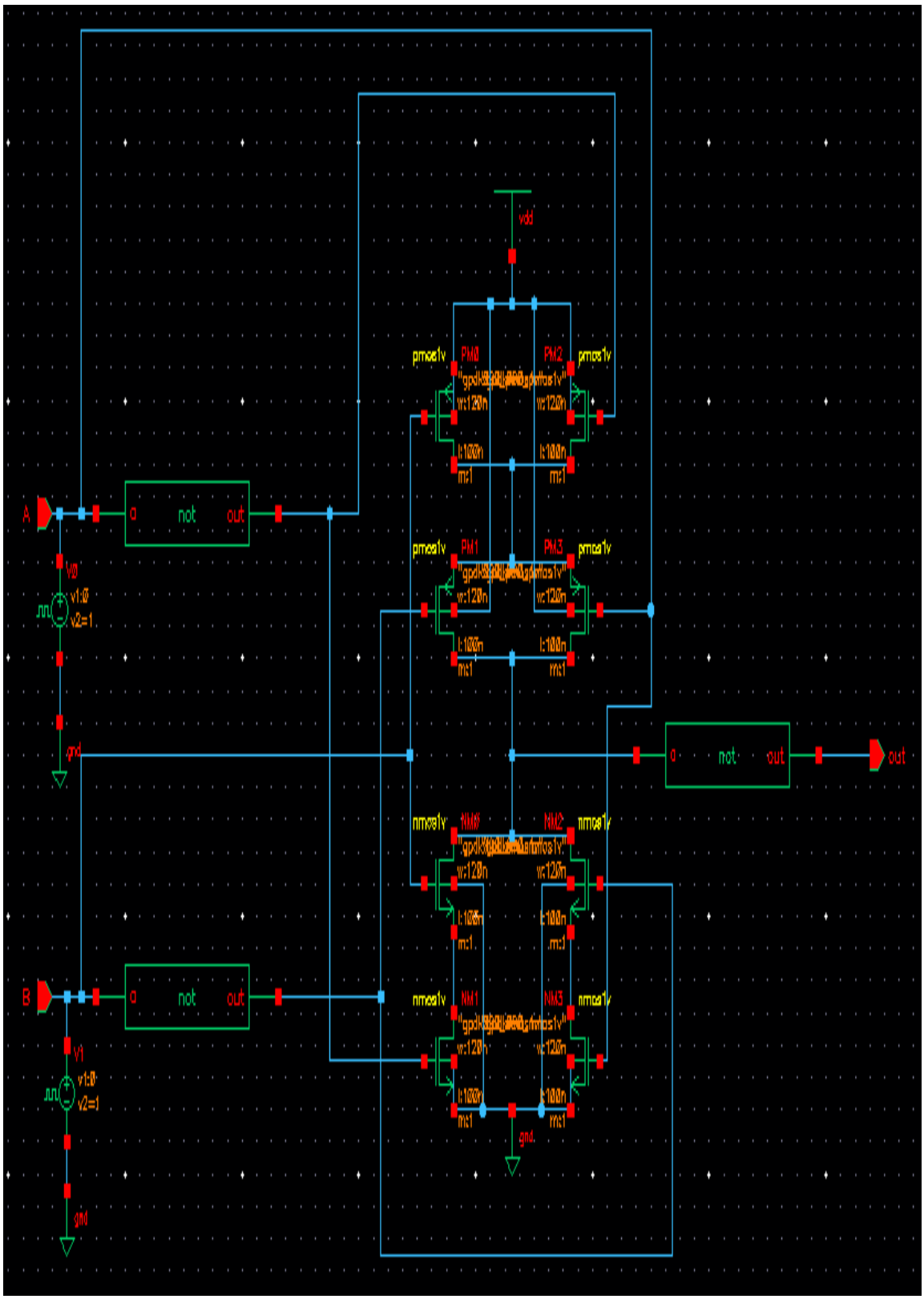


Fig. 8: XOR Gate Using MGDI Technique

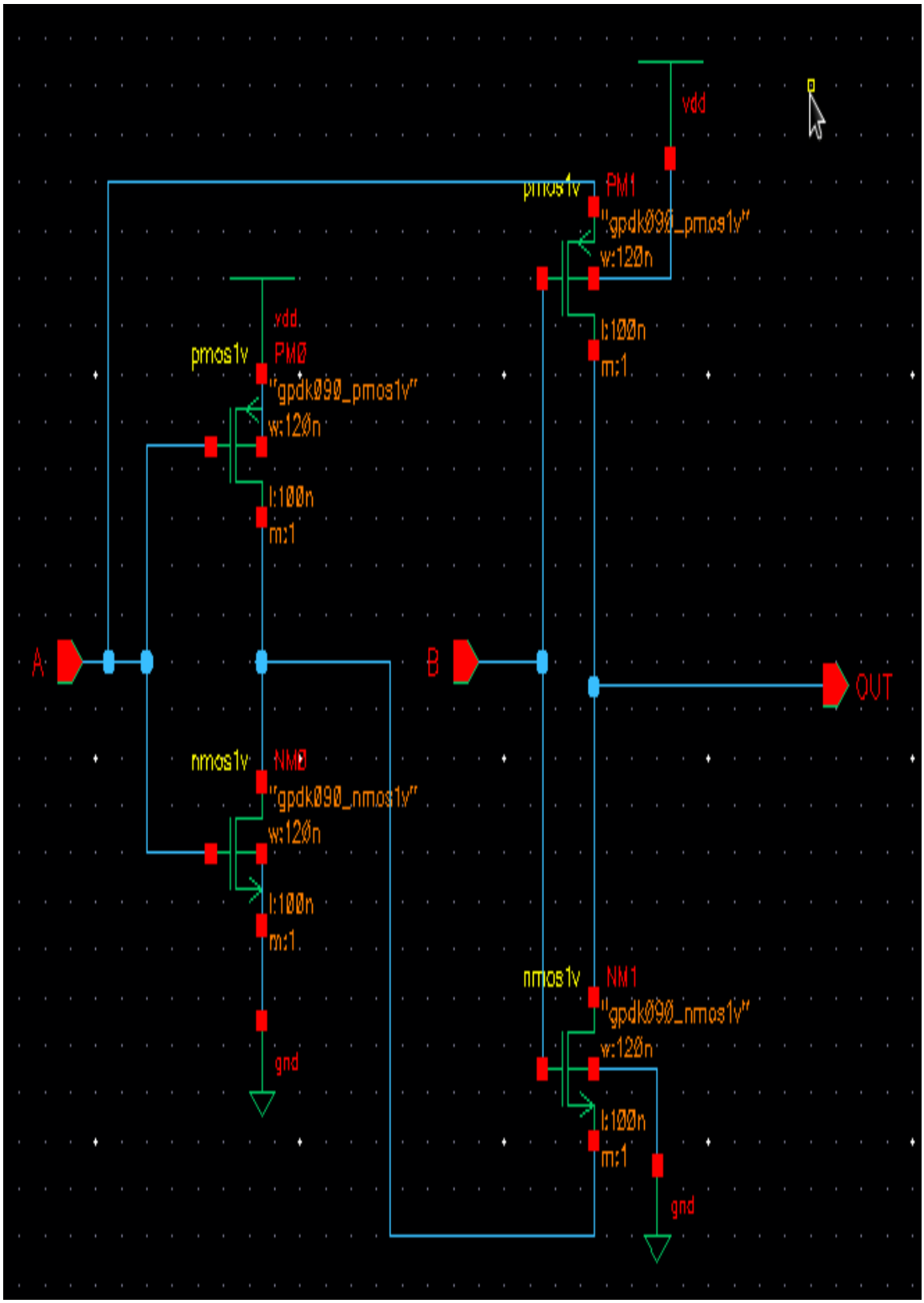


Fig. 9: Waveform of Binary to Gray Code Converter Using CMOS Logic

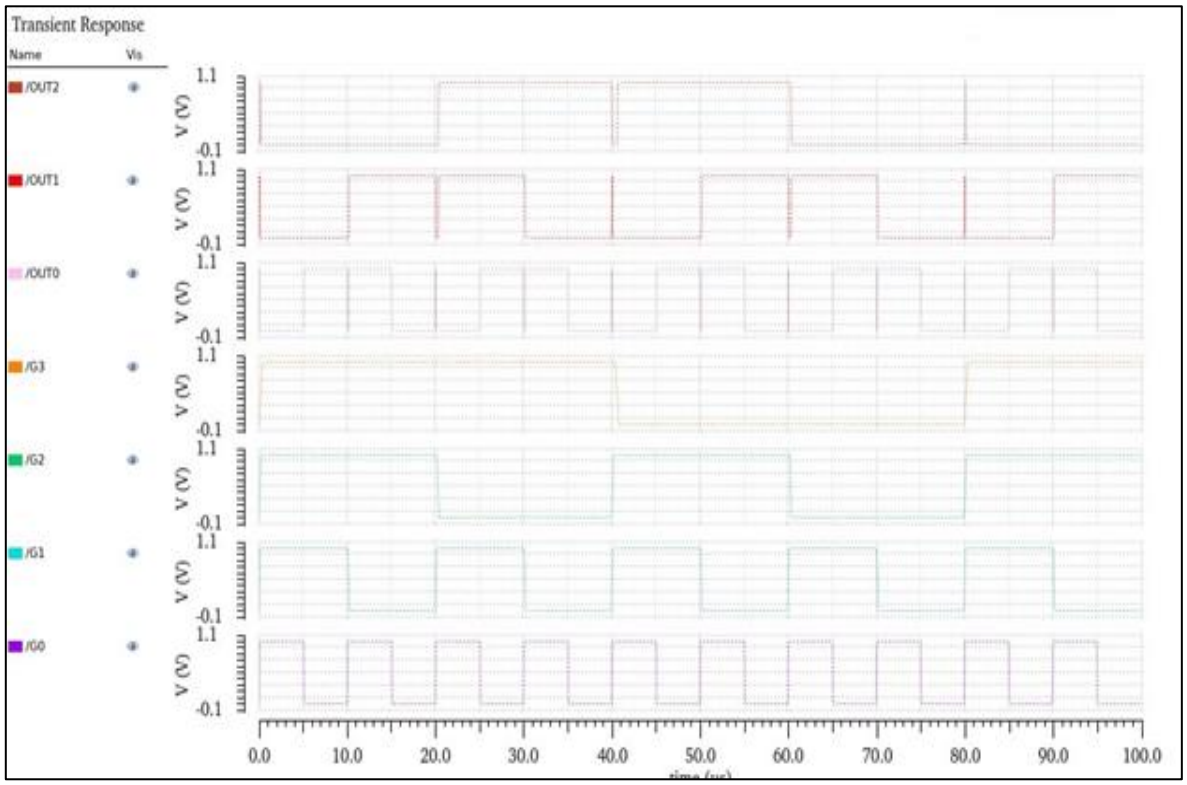
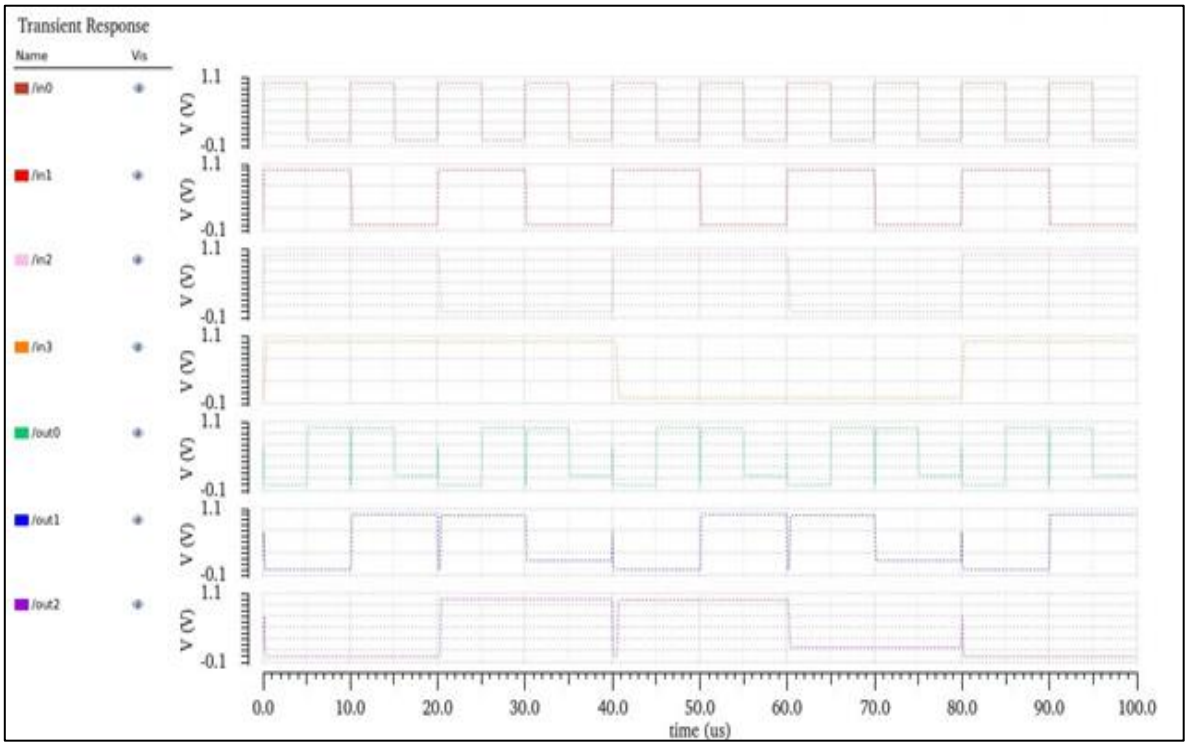


Fig. 10: Waveform of Binary to Gray Code Converter Using Modified GDI Technique



As there are 3 XOR gates in a binary to gray code converter, so, to decrease the number of MOSFETs, reduce power consumption and area, it is important to focus on the design of XOR gate with minimum number of MOSFETs. Using MGDI technique, the number of MOSFETs can be reduced to a significant amount in XOR gate as shown in Fig. 7 and Fig. 8. In the CMOS logic, 14 transistors are used, whereas in MGDI technique only 4 transistors are used to get the desirable output for XOR Gate.

For the design of binary to gray code converter, circuit diagram of Fig. 6 is used; the XOR block is replaced by respective XORs of CMOS logic (Fig. 7) and MGDI technique (Fig. 8).

4.1 Simulations

To check the performance the proposed code converter, transient analysis is performed, and total power dissipation is calculated. The transient analysis is an analysis which measures the circuit's response over a period of time defined by the user. In this, input is provided with high and low pulses of different pulse width and rise and fall delay. The waveform generated after the simulation is analyzed to look at the accuracy of proposed schematic. The waveforms generated for both CMOS logic and MGDI technique for the Binary to Gray code converter are shown in Fig. 9 and Fig. 10.

In Fig. 9, G3, G2, G1, G0 are 4-bit input values and OUT2, OUT1, OUT0 are the output values where OUT3 is same as G3. In Fig. 10, in3, in2, in1, in0 are 4-bit input values and out2, out1, out0 are the output values where out3 is same as in3. From Fig. 9 and Fig. 10, the waveforms generated through the CMOS logic and MGDI technique, it can be seen that output logics are correct in both. But for some input values in MGDI technique, the output generated is not able to give strong '0' and strong '1' logic values. Hence, some of the output waveforms are degraded to some extent.

4.0 Results and Discussions

4.1 Power dissipation

Broadly, there are two types of power dissipation in MOSFET circuits, namely Dynamic power dissipation and Static power dissipation. The dynamic power dissipation occurs due to two types of current flow during the functioning of the circuit. The first one is the charging and discharging current to charge and discharge the output load capacitances during the swicthing of the inputs. The second one is the short circuit current that flows from power suply to ground through switched ON PMOS and NMOS transistors for a short while, as the input signal transitions from either low to high logic or vice versa [5]. The static power dissipation occurs due to leakage currents in the transistors in nominally off state and sub-threshold currents. The diode formation takes place in the MOS structure where the reverse bias PN-junction leakage between the source/drain and substrate occurs, and it becomes more significant if the temperature rises. The sub-threshold currents flow due to charge carrier diffusion between source and drain when gate voltage is slightly less than or equals to the threshold voltage of transistor. The total Power Dissipation is the sum of both dynamic and static power dissipation. The total power dissipation was measured during the transient analysis of the circuits by applying a pulse input signal at the input node continuously.

4.2 Number of transistors

The number of transistors needed to design a particular logic gate or code converter can be counted from the schematics shown in Sections.

4.3 Comparison of CMOS logic and MGDI technique

Table 3 shows the comparison of both CMOS logic and MGDI technique in terms of number of transistors and total power dissipation for various gates and binary to gray code converter. The number of transistors reduce considerably in the circuits designed using MGDI technique as compared to CMOS logic. Even in the case of basic gates like AND, OR, the number of transistors in MGDI technique is one-third of that of CMOS logic, though the number of transistors remain same in case of complemented logic such as inverter, NAND, NOR in both cases. Considerable difference in number of transistors is seen for a small circuit like binary to gray code converter; the number of transistors needed in MGDI technique is only about 28% than that in CMOS logic.

Similarly, much better results can be seen for power dissipation in circuits designed using MGDI technique in comparison to CMOS logic. For most circuits, the power dissipation using MGDI technique

is between 30 to 40% of that of power dissipation using CMOS logic. In fact, for NOR and NAND gates, power dissipation is just 3% and 19% respectively in Modified GDI as compared to CMOS logic.

Table 3: Performance Evaluation of Logic Functions

Logic Circuit	No. of Transistors		Total power dissipation in nW		Power dissipation %
	CMOS	Modified GDI	CMOS - PD1	Modified GDI-PD2	PD2/PD1 (%)
Invertor	2	2	41.97	12.56	29.93
AND gate	6	2	60.61	23.59	38.92
OR gate	6	2	45.01	16.23	36.06
NAND gate	4	4	47.58	9.21	19.36
NOR gate	4	4	23.9	0.804	3.36
Binary to Gray Code Converter	42	12	408.2	125.6	30.77

Table 4: Performance Evaluation of Logic Functions

Logic Circuit	No. of Transistors		Total power dissipation in nW		Power dissipation %
	CMOS	Modified GDI	CMOS - PD1	Modified GDI-PD2	PD2/PD1 (%)
Invertor	2	2	41.97	12.56	29.93
AND gate	6	2	60.61	23.59	38.92
OR gate	6	2	45.01	16.23	36.06
NAND gate	4	4	47.58	9.21	19.36
NOR gate	4	4	23.9	0.804	3.36
Binary to Gray Code Converter	42	12	408.2	125.6	30.77

5.0 Conclusions

This paper exhibits the performance analysis of basic logic functions and a code convertor using Modified Gate Diffusion Input technique as compared to CMOS logic. The performance measures were total power dissipation and the use of the number of MOSFETs in conventional CMOS logic and MGDI technique. From the analysis, we observed not only there is significant amount of decrease in total power dissipation and reduction in the use of number of MOSFETs but also the transient analysis provided correct values for schematics proposed in MGDI Technique. Only limitation occurred was it was not able to produce a strong '0' or '1' logic at the output for certain input value combinations. The complete designs and simulations were carried out using 90nm technology at 1.0 V in Cadence Virtuoso Tool. Therefore, Modified GDI technique comes out to be a good substitute for existing CMOS technology that can be used in high performance and more complex digital circuits and designs.

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