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Single-Bit Architecture Cache Memory Design Analysis

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ABSTRACT

This work includes the design of voltage and current difference latches and low-power cache memory for a single-bit processor core architecture. To save power, the single-bit cache memory uses voltage differential sensing amplifiers.

Keywords: *Voltage differential sense amplifier (VDSA); Write Driver Circuit (WDC); Current Latch Sense Amplifier (CLSA); Differential Sense Amplifier (DSA); Six Transistors Static Random-Access Memory (STSRAM); Latch Sense Amplifier (SA).*

1.0 Introduction

Many mobile gadgets and systems that work together demand batteries [1]. The single-bit cache memory on the chip, which takes up 60 to 70 per cent of its surface area, is where the data is kept. As chip utilization rises, CPU speed declines. As demand for VLSI systems increases quickly, low-speed, low-power memory circuits are designed to keep up. The number of transistors added or subtracted impacts how quickly a chip fails for each. The fundamental premise of the paper is that sensory stimulation improves cognition. According to predictions, memory cache will eventually occupy more than half of high-performance microprocessor transistors [2]. SRAMC semiconductors are renowned for functioning effectively in noisy situations. Due to this, high-performance computers with lower electrical requirements have become more popular. With SRAMC, smaller memory cells are not a concern. This means the user can utilize the entire amount of RAM on the gadget. A city grows and evolves more quickly and drastically than other areas. There is a SA, which is sensitive to high frequencies, inside each SRAMC memory block. SA typically takes into account things like memory access times and power consumption. In memory systems, side circuits [3,4] play a key role. By digitizing the analogue levels in peripheral Boolean networks, the SA can hasten data transmission from one memory cell to the next in the logic circuit [5].

1.1 Single bit architecture cache memory design

This section covered the operation of single-bit cache memory. The concept is only partially illustrated in Figures. 1 and 2. The Cache Memory Design for Single-Bit Architecture includes WDC, STSRAM, and other sense amplifiers, including voltage differential and current latch sense amplifiers [11,12].

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Figure 1: Single Bit STSRAM VDSA Architecture

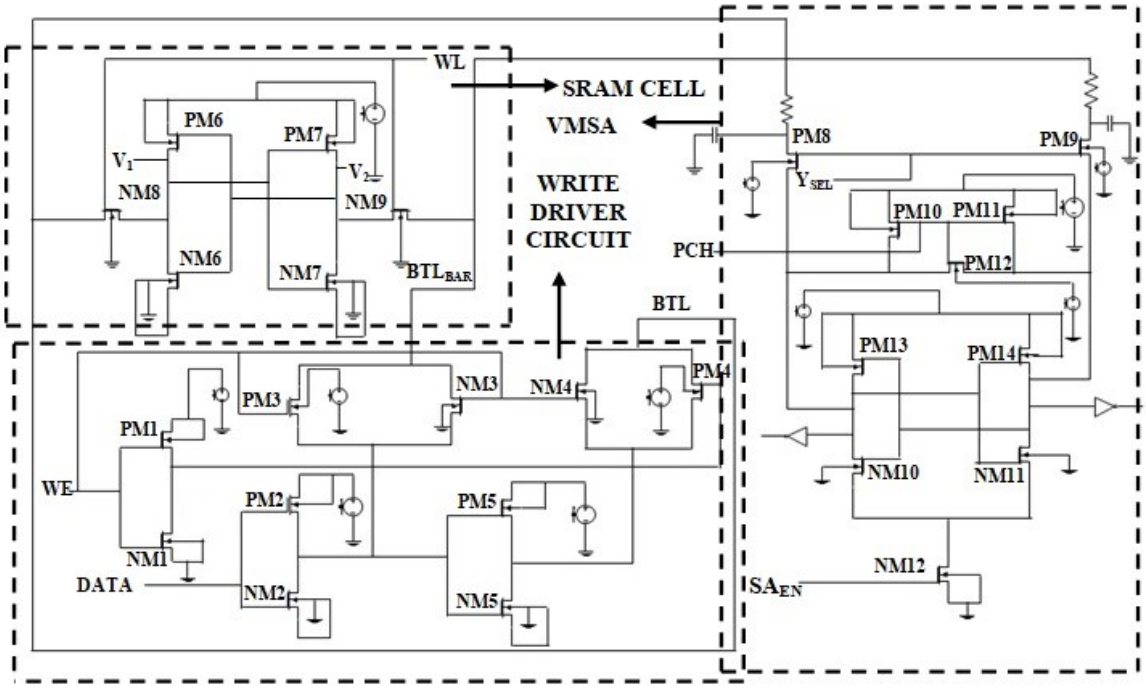
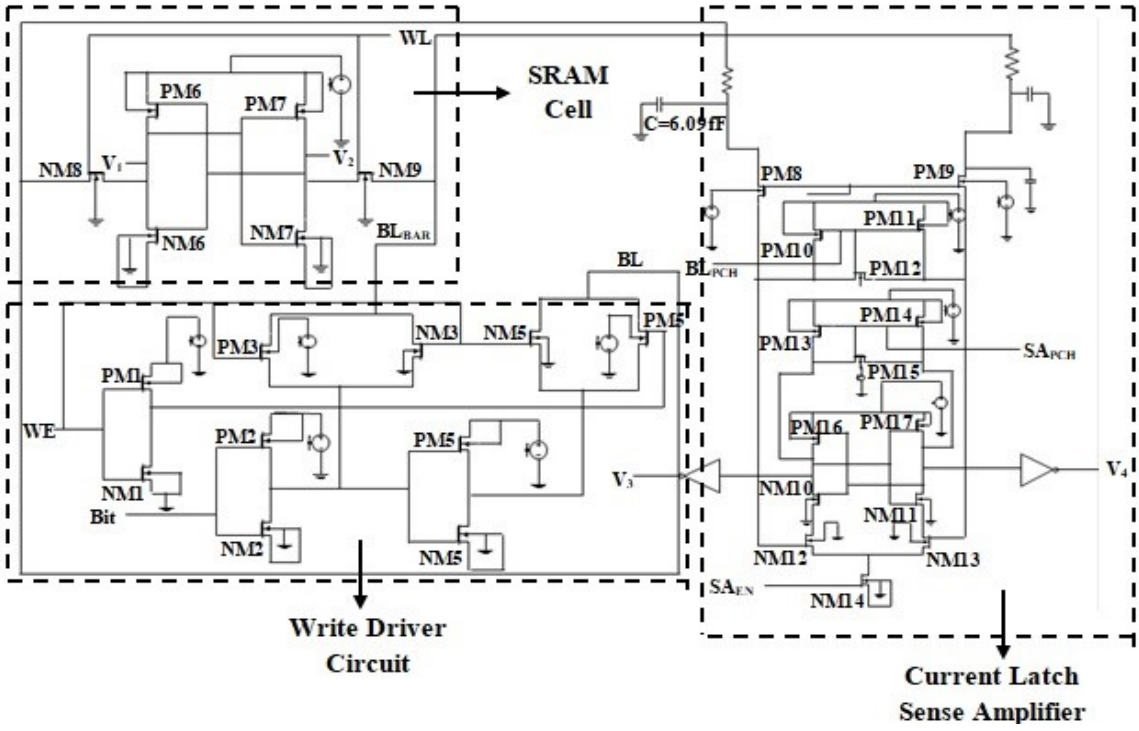


Figure 2: Single Bit STSRAM CLSA Architecture



1.2 WDC

The WDC is seen in action in Figure 3. The STSRAM write driver quickly drains each bit line from the pre-charge stages once the write margin has been achieved.

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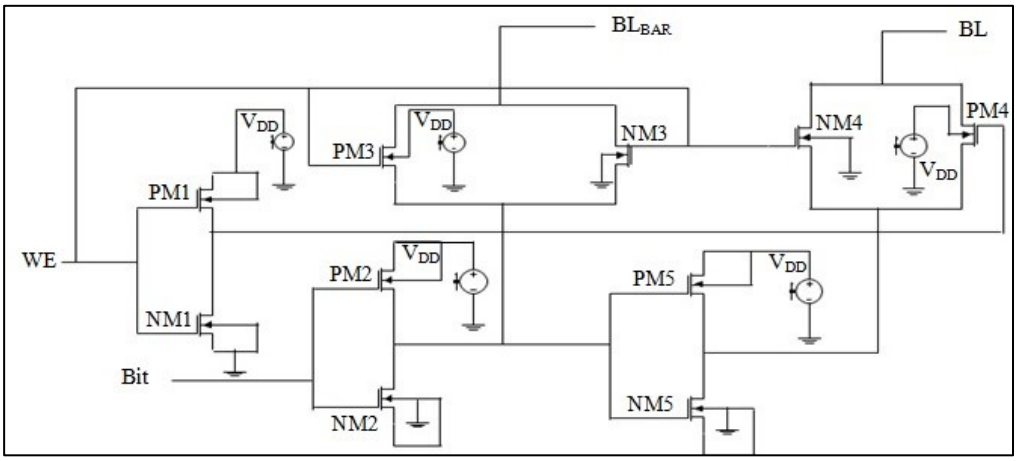
Figure 3: WDC

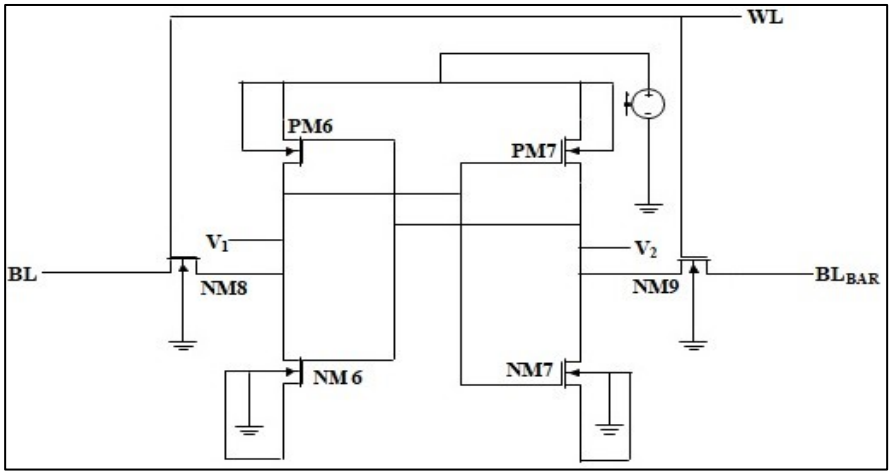


The write enables (WE) signal, which activates the write data converter, is typically sent over the bit line. A pre-charge takes place before the full-swing charge to the ground (WDC). Every PMOS and NMOS in the WDC's stock are now in use. Every PMOS has a PMOS for PM1, PM2, PM3, PM4, and PM5 (NM1, NM2, NM3, NM4, and NM5). Depending on the data, one of the transistors may be PM1 or NM1.

1.3 SRAMC

It works well for tasks that don't require much power or voltage. A latching circuit tracks each bit. Driving (M1 and M2) and drawing up transistors are shown in Figure 4. (PMOS). There is more noise margin with these bit lines. It is unnecessary to reload DRAM cells [15, 16] while the power is still on. The performance of an SRAM is influenced by transistor size.

Figure 4: SRAMC



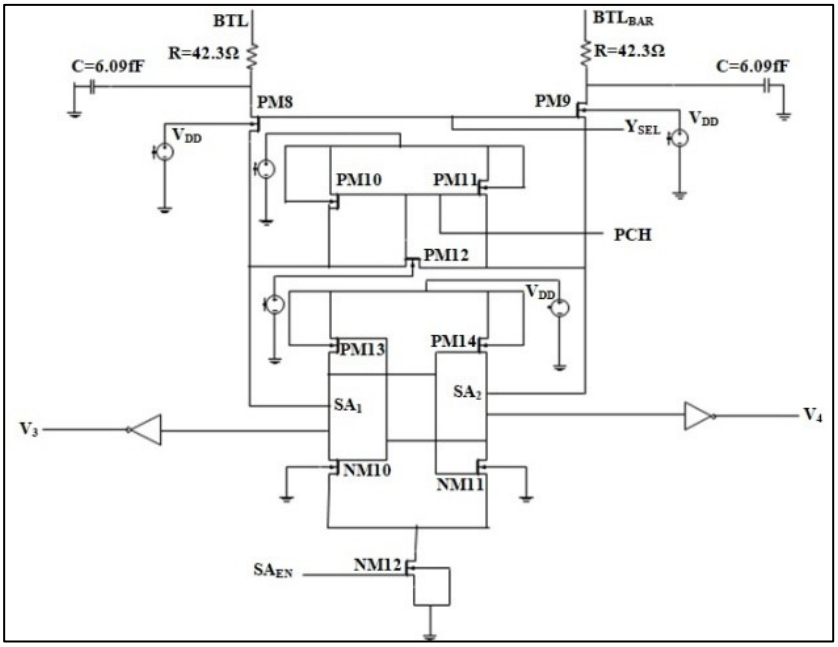
1.4 DSA and LSA

The sensing amplifier causes the voltage differential between the read-access bit lines to increase. The overall quality of the digital output depends on the amplification. More transistors are necessary to break up lengthy data lines. The metal is stronger as a result.

1.5 VMSA

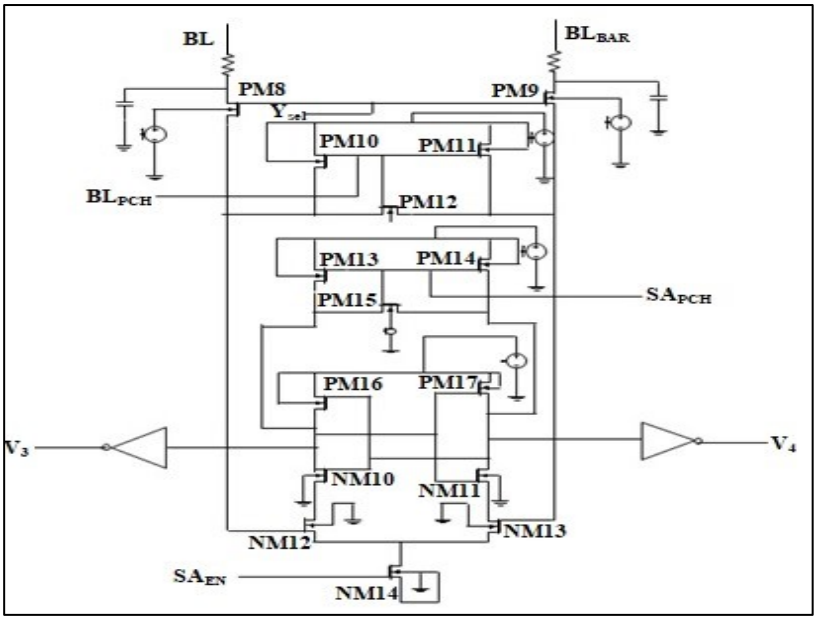
The amplifier receives power from the voltage difference between the two-bit lines. A cross-connected inverter converts the initial voltage difference between the bit lines into full swing output. The cell column bit lines multiply the BTL and BTLBAR inputs. The sensory boost, which also activates the memory cell in P1 and the sensory boost in P2, is triggered by N3. To shield the internal nodes of the sensor amplifier from outside influences, output inverters are necessary [17,18].

Figure 5: VMSA



1.6 CLSA

Figure 6: CMSA



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The internal structure of a current latching amplifier is shown in Figure 6. The circuit is covered in great detail in [19, 20]. The CLSA's SA3 and SA4 observe the voltage variations on the bit lines. SA1 and SA2 emerge each time SAEN ascends. A positive feedback loop is established when the sensing amplifier's level is low enough to activate the PMOS device PM16. SA2 splits its inputs and outputs to lessen chargeback interference.

2.0 Results Analysis

The SAEN and WL are both high in Figures 7 and 8, even though the VDSA and CLSA are in reading mode. Only V3 and V4 can access STSRAM data while the SA is present.

Figure 7: VMSA O/P

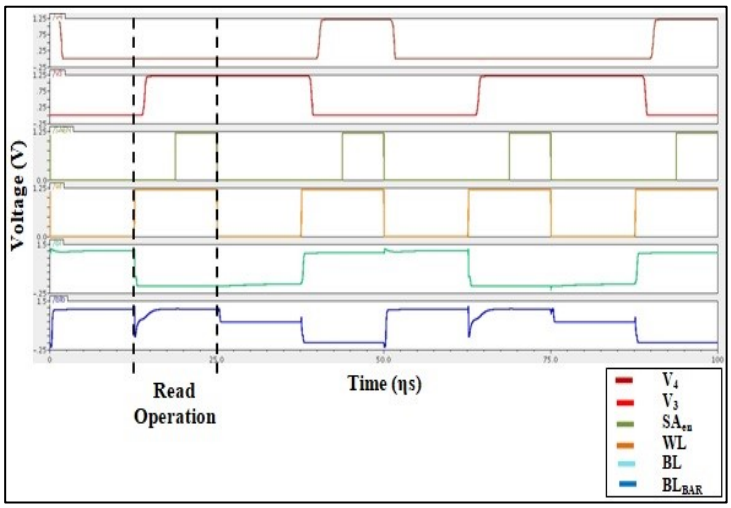

Figure 8: Current Latch Sense Amplifier Output Waveform

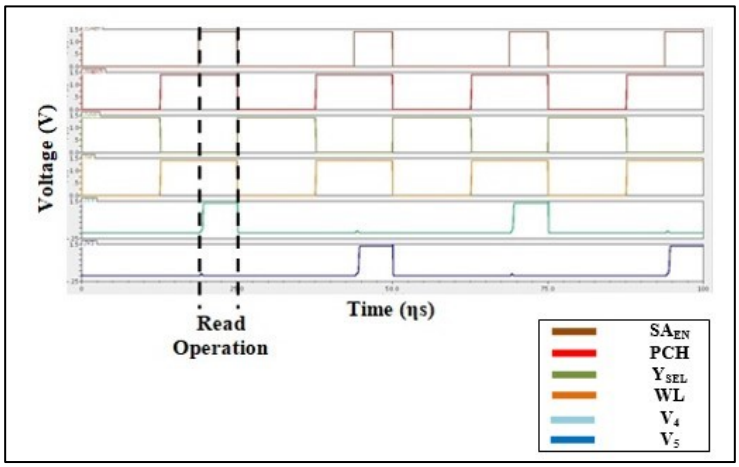

Table 1 shows that the power consumption of single-bit STSRAM VDSA devices decreases when resistance increases. The cache memory in Table 2 uses a single-bit STSRAM CLSA design, which uses less power.

Table 1: Different Cache Memory Design Parameters are Employed for Single Bit STSRAM VDSA Architecture

Parameters	Single Bit STSRAM VDSA Architecture	
	Delay in Sensing	Consumption of Power
R=42.3Ω	25.25ηs	13.16μW
R=42.3KΩ	25.25ηs	11.34μW

Table 2: Design considerations for Single Bit STSRAM CLSA Architecture Cache Memory

Parameters	Single Bit STSRAM CLSA Architecture	
	Delay in Sensing	Consumption of Power
R=42.3Ω	25.25ηs	81.78μW
R=42.3KΩ	25.25ηs	30.12μW

3.0 Conclusion

It is feasible to enhance the cache memory properties of voltage differential sense amplifiers and current latch sense amplifiers by increasing the resistance (R) in the design. The number of transistors, the amount of power consumed, and the sensor's response time. One strategy for cutting power usage is to use single-bit memory blocks. A voltage differential sensing amplifier and a static random access memory cell with six transistors are used to create a single-bit cache memory.

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