DC Voltage Balancing Technique for CMI-based STATCOM: A Generic Control Approach

Rasiyawan Yadav* and Preet Lata**

ABSTRACT

This article provides a generic technique for per phase DC bus voltage balancing that might be used in a CMI based STATCOM. The STATCOM system parameter model and the conventional control technique are examined first. A per phase DC bus voltage balancing mechanism is detailed using a dq/abc park transformation and the loop-gain shaped control design technique. This approach aims to maintain a constant DC bus voltage. The dc capacitor may be controlled globally by a proportional resonant controller. A controller that rejects disturbances may be used to regulate clustered loads. By facing a number of challenging tasks at the point of aggregate generally, including balancing the DC voltage and accounting for reactive power. If these problems can be handled, the system's supremacy could be increased. This article describes the general control arrangement in order to increase the system's reliability. This system may accomplish reactive power compensation and dc link voltage balancing by using the nine-level cascade multilevel inverter as STATCOM. One particular topic has been emphasised repeatedly throughout the text.

Keywords: CMI; STATCOM; Facts Devices; DC Voltage.

1.0 Introduction

For many years now, reactive power compensation has already been widely used as a reliable and efficient method of controlling electric power grids. Fast speed, a small footprint, and low harmonics are just a few of the benefits of the STATiC synchronous Compensator (STATCOM), a novel reactive power compensator based on power electronics converter technology [1]. To this day, H-bridge cascaded STATCOM still faces two technological hurdles. To begin, the compensation performance is significantly impacted by the present loop control strategy. However, the compensatory effect is diminished due to various less-than-ideal aspects. These include the narrow bandwidth of the output control loop, the delay introduced by the signal recognizing circuit, and the process of generating the reference command current [2]. Second, since H-bridge cascaded STATCOM is a complex system with many H-bridge cells in each phase, the dc capacitor voltage discrepancy issue, which is caused by different power losses amongst cells, having switched patterns in different cells, parametric uncertainties of active and passive elements inside cells, will affect the reliability of the system and could even cause it to fail. Therefore, several studies have attempted to uncover answers for these issues [3].

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*Corresponding author; Manager, Ntpc Ltd., India (E-mail id: rasiyawanyadav@ntpc.co.in)

**Principal Investigator(Women Scientist), NIT Kurukshetra, India (E-mail: preetklata@gmail.com)

This article introduces the CMC STATCOM's generic approach to per-phase DC-bus voltage balancing. To begin, we examine a generalized STATCOM model and the control mechanism it currently employs. Based on the loop-gain shaping and the dq/abc park transformation, a per-phase DC-bus voltage balancing system is developed [4]. Adding the suggested control to the DSP controller is straightforward and requires essentially no more computational resources. In general, series FACT controller and shunt FACT controller are the two types of FACT controllers available [5]. Through compensating for transient drops and spikes, series controllers enhance power system reliability. When it comes to transmission and distribution, shunt FACT controllers are often used because of their quick reaction time and low overall cost. The ability to regulate power from a few kilovolts to many megavolts makes multilevel inverters a powerful tool for STATCOM applications in transmission systems [6]. Cascade multilevel inverters (CMI) are becoming more popular due to their many advantages over other types of multilevel inverters. These include neutral point clamped multilevel inverters, flying capacitor multilevel inverters, and CMIs.

Compared to other multilevel inverter topologies, including flying capacitor and diode clamped multilevel inverter, its modular construction, capacity to attain at greater output voltage and power level, and fewer necessity of components set it apart [7].

Figure 1: Schematic of a CMI-based STATCOM
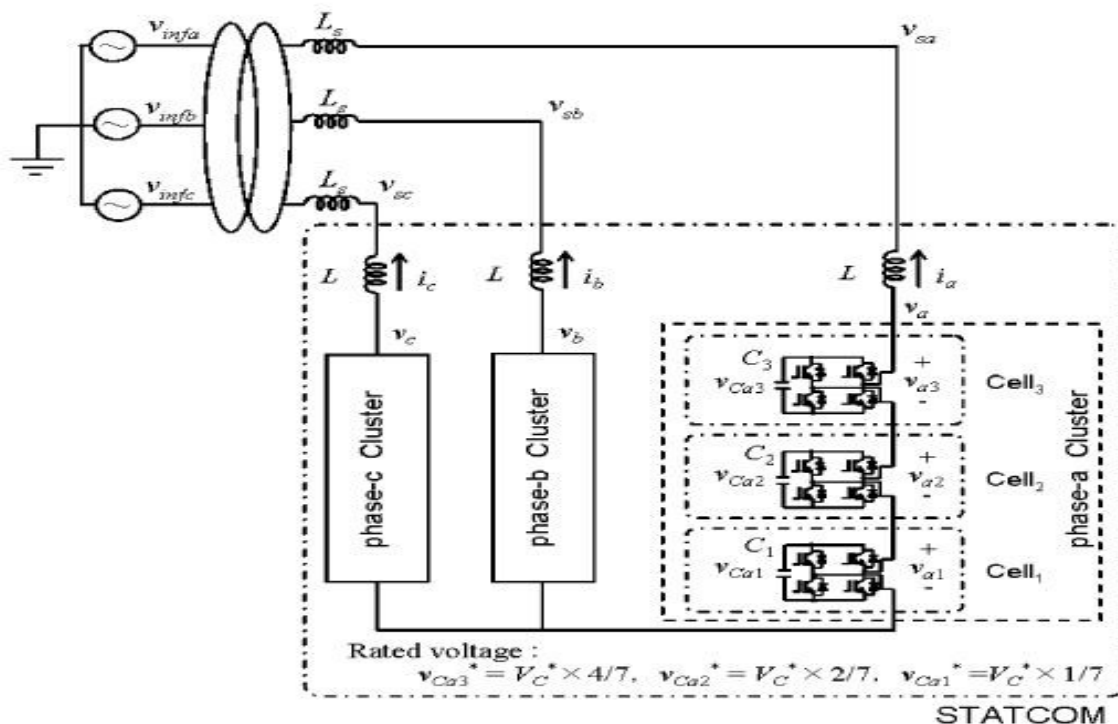

2.0 Configuration of CMI based STATCOM

It is possible to directly manage the current flowing via STATCOM in order to either absorb or deliver the required reactive current in order to achieve the objective of dynamic reactive current compensation [8]. Because of improvements made to the power quality of the grid, only active current is supplied by the grid.

2.1 Mathematical modling

Determining the steady-state and dynamic modelling equations is a crucial step in developing an acceptable control strategy for CMI-based STATCOM. In order to assess the system as a whole, mathematical modelling is required [9]. By simulating a power converter coupled to the transmission and distribution network through reactance, CMI-based STATCOM may be analysed. Where Vs is the voltage of the power system, Vc is the voltage of the STATCOM, Ic is the current drawn by the STATCOM, and R and L are the total resistance and inductance between the source and the STATCOM used to hold the voltage difference, we get the single-line diagram of a CMI-based STATCOM, as shown in Figure 2.

The circuit's settings are shown in Table I below. Each phase of this cascade multilevel inverter's three-phase, nine-level output voltage is generated by a series-connected H bridge string. The dc side just uses the dc capacitors and a voltage sensor for power and has no external connection. The STATCOM ac pulse width modulation (PWM) voltage has a higher frequency than the grid's sinusoidal voltage, thus an ac inductor is used in each cluster to smooth down the voltage [9]. As an additional benefit, the ac inductor helps eliminate PWM-induced ripples at the switch. Taking into account the intricacies of real-world industrial fields, spiking current and over loading might be issues when choosing an IGBT [10].

Figure 2: CMI based STATCOM – Single Line Diagram
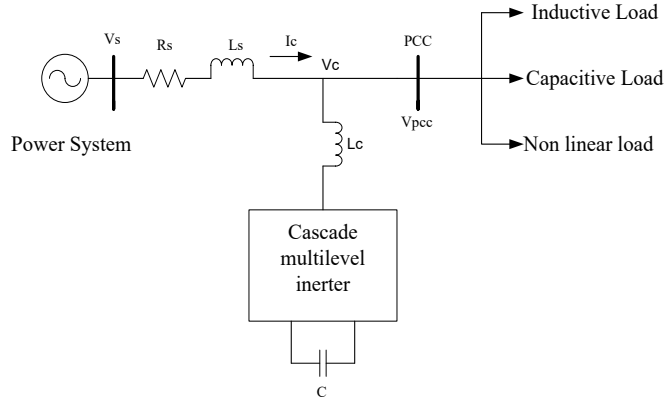
Several assumptions of the CMI-based structure, including the system's modularity, the identical voltage level of each capacitor, and the same value of the DC link capacitor, are used in conjunction with Kirchhoff's law to establish the dynamic model of the system [11].

This is the equivalent circuit as the one in Figure 8.

$$L\frac{dI_S}{dt} + R.I_S = V_S - V_C \qquad \qquad \text{...(1)}$$

Because of the disparity between the network voltage and the STATCOM voltage, the coupling settings allow STATCOM to generate its own current, as shown below.

$$L\frac{d}{dt}\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + R\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} - \begin{bmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{bmatrix} \qquad \qquad \text{...(2)}$$

Three-phase source voltages are denoted by Vsa, Vsb, and Vsc, whereas STATCOM voltages are denoted by Vca, Vcb, and Vcc.

2.2 DC bus voltage balancing

A cascading multilayer inverter is constructed up of H bridges that are connected in series with various DC capacitors. These bridges make up the inverter's fundamental building elements. Unbalanced DC voltage is a problem, and it's caused by differences in the parallel loss that are associated with each H bridge of the CMI. Unbalanced DC voltage has a number of unfavorable effects on the scheme, along with an increment in the harmonic currents of the current and a decline in the reliability of the synthetic output waveform from the converter [12]. Both of these effects are caused by the system's inability to properly balance the DC voltage. When the number of levels in a CMI increases, the regulation of the DC voltage that exists between those levels becomes a more important financial and logistical consideration [13].

**Table 1: The Experimental System's Circuit Parameters**

Grid voltage	11 kV
Rated reactive	120 Kvar
AC inductor	10 mH
DC capacitor	4.68 mF
Number of Cells/Phase	4
PWM carrier frequency	1 kHz
Reactive Current	9 Amp

3.0 Control Architecture

There are only two degrees of freedom in the primary control loop, which are denoted by the symbols Idref and Iqref in Figure 2. These symbols are used to regulate the active current and the reactive current, respectively. Because Iqref is utilised for the creation of reactive power, the Idref can only be used to manage the approximate value of each DC bus's voltage [14]. The voltage loop and the Idref channel are responsible for ensuring that the overall DC bus voltage is balanced. However, the DC bus voltages of each phase are not regulated. When the STATCOM has no power losses, no active power is exchanged between the STATCOM and the AC system, and only reactive power is provided by STATCOM. This only occurs if the parameters and trigger signal of each H Bridge are identical [15].

Synchronization circuits that use a phase locked loop determine both the phase difference and the reference frequency [16]. Voltage and current measurements must be taken at the point of connection in order to perform the transformation from abc to dq in a vector. Two separate controllers, one for each DC bus, make up the DC regulator. DC link voltage within each phase and between phases must be balanced by these controllers. As shown in Figure 2, the dc voltage regulator, ac voltage regulator, and PWM modulator will work together to provide a tunable switching command that will be sent to the CMI STATCOM. Using modulation schemes, such as Phase-shifted pulse width modulation (PWM), simplifies the operation of the control system. Reason being, when more cascade bridge cells are added to a cluster, the control system becomes more complicated [17].

Figure 3: CMI-based STATCOM Controller
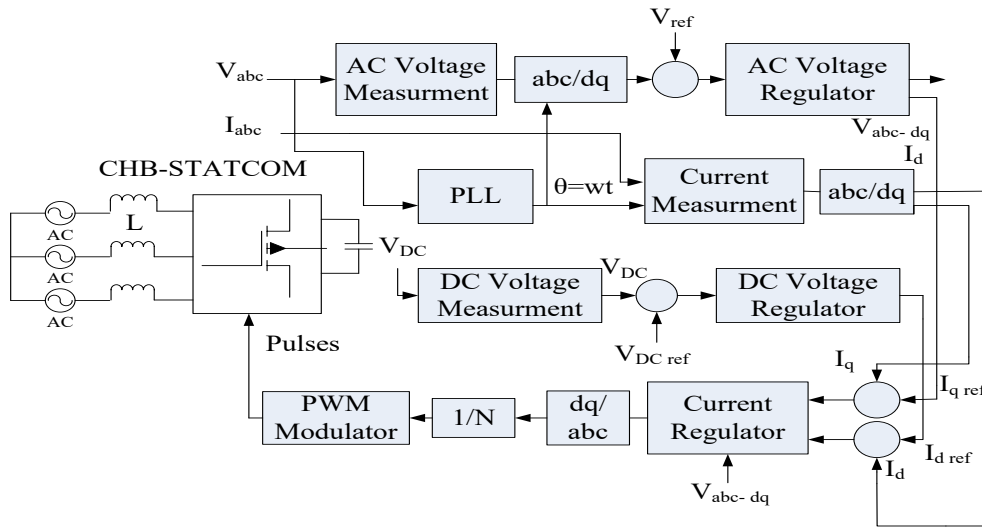
4.0 Simulation Results

The simulation results have been used to demonstrate the system's superiority by demonstrating its well specified dynamic performance, which includes meeting power requirement at the load side. Using a nine-level cascade multilevel inverter, which can provide an approximation of sinusoidal voltage in the form of a stepped 17-level output line voltage waveform, research has been conducted on a STATCOM. The control approach for a nine-level CMI is implemented in a simulation in this chapter, and the results are presented.

Figure 4: Waveform of Voltage and Current at the PCC in Capacitive Mode (a) and Inductive Mode (b)
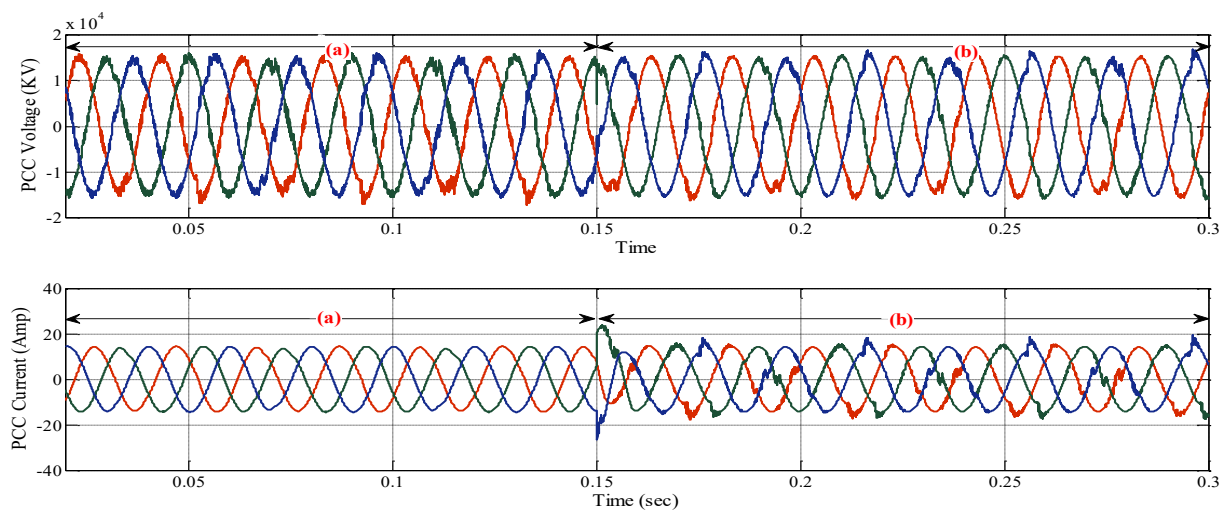
Simulation parameters are listed in table1 according to the mathematical model of STATCOM. Figure 4 shows the voltage and current waveform at the point of common coupling in both capacitive mode (a) and inductive mode (b) with step change at 0.15 sec. The grid and

STATCOM voltage at the value of same magnitude can be achieved by keeping the coupling parameter between the grid and STATCOM at the level of its optimum value with a step change at 0.15 sec as shown in Figure 5. Figure 6 indicates the dynamic performance of CMI based STATCOM by the tracking in between reactive current reference (I_q^*) and reactive current (I_q) supplied by STATCOM from capacitive mode to inductive mode with a step change at 0.15 sec. The STATCOM supplied reactive current viewed some oscillations or spikes when the loads are changed from one mode to another mode. In contrast, STATCOM is accessible to absorb reactive current from power system to operate in inductive mode while it delivers reactive current to the power system in capacitive mode.
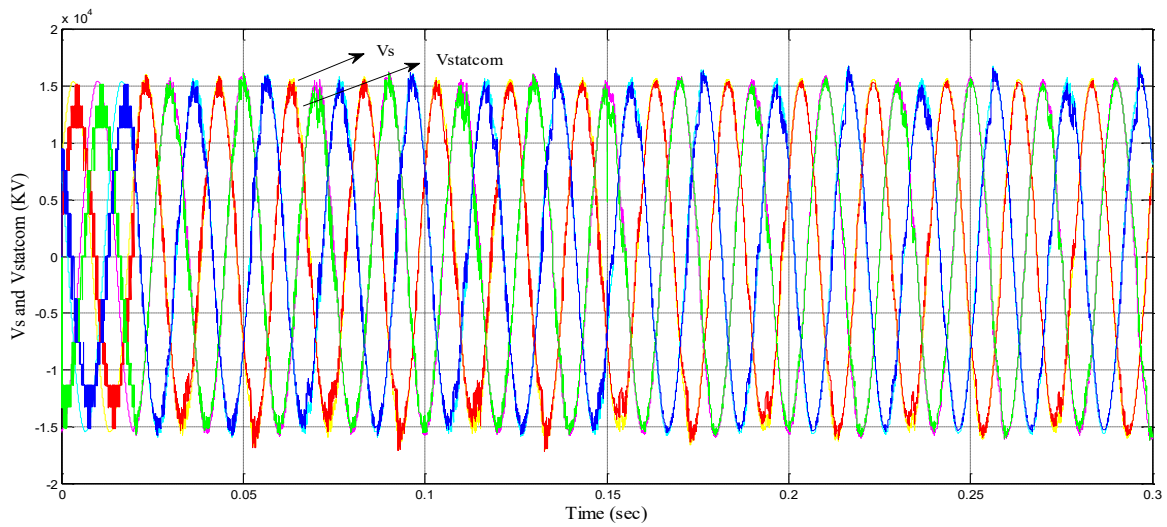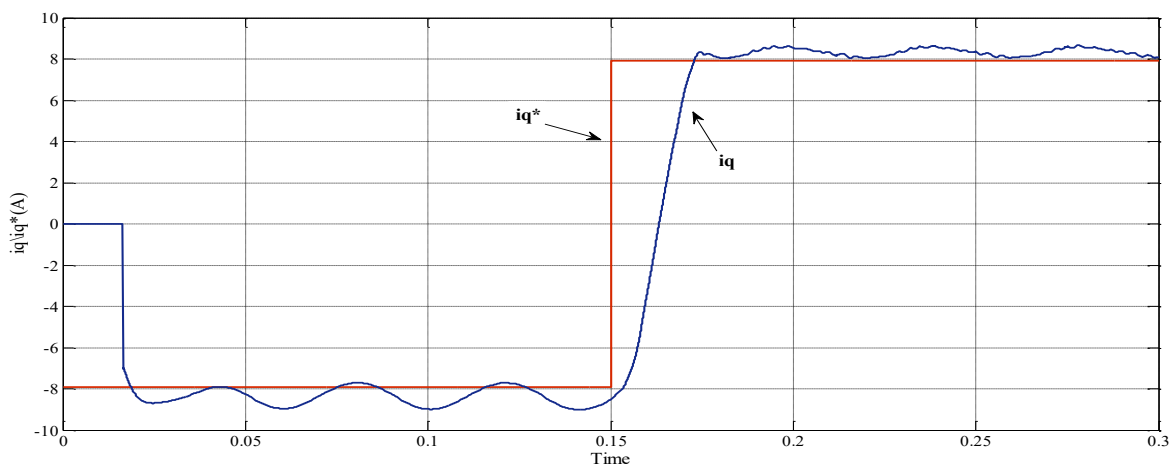
Figure 5: Grid (Vg) and STATCOM Voltage (VSTATCOM)

Figure 6: Reactive Current Component Tracking

5.0 Conclusion

The simulation results validate the basic working concept of the given nine-level cascade multilevel inverter. In order to achieve nine levels of CMI, multicarrier PWM is used. Comparisons

have been made between the different modulation techniques to examine the THD performance of phase voltage and line voltage. Throughout this article, we have covered the major uses of CMI. The study delves into the inner workings of STATCOM, a communication system that relies on a multilayer H-bridge converter set up in a star configuration. This study presents a CMC-based STATCOM's generalised per-phase DC-bus voltage balancing technique. According to the dq/abc park transformation and the resulting open-loop transfer function

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