JFSA

Journal of Futuristic Sciences and Applications
Vol. 4(2), Jul-Dec 2021, pp. 31-38
doi: 10.51976/jfsa.422105
www.gla.ac.in/journals/jfsa

The Architecture of Memory for Core Processors

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ABSTRACT

The effectiveness and storage capacity of single-bit cache memory have been investigated. Write driver circuit, random access memory cell, and current mode detector make up the single-bit cache. Using various strategies, such as power-saving components like current mode sensing amplifiers and static random access memory cells, memory systems with just one bit of cache can use less power. To save power, substitute a forced stack and a current mode detecting amplifier for a single-bit cache.

Keywords: *Current Mode Sense Amplifier (CMSA); Single Bit SRAM CMSA Architecture (SBSCMSA); Sense Amplifier (SA); Static Random-Access Memory Cell (SRAMC); Write Driver Circuit (WDC).*

1.0 Introduction

As transistors get smaller, large integrated circuits can have more circuits and function better. Transistors in most integrated circuits are connected by wiring [1-4]. The wiring within a semiconductor is referred to as the "global interconnect on-chip." Other global linkages, including those connecting cache memory to CPUs, are emerging alongside breakthroughs in submicron VLSI technology. How long it takes to make depends on how many connections a chip has globally [5-7]. Transceivers and signalling protocols enable faster message transmission. The recordings of sense amplifiers used as connection receivers allowed for this discovery. A combination of the SRAMC and sense amplifier has also been suggested [8–10].

1.1 Power reduction techniques

The requirements of a circuit are met while using less electricity [11].

1.1.1 Sleep transistor technique

State-destructive operations can harm PMOS and NMOS sleep transistors connected to the supply voltage or ground. The same technology is known by the names VDD and gated-ground [12]. Sleep semiconductor technology lowers the power used during sleep by separating logical networks from sleep transistors (see Figure 1).

1.1.2 Forced stack technique

Figure 2 illustrates the forced stack. Costs can be further decreased by stacking transistors. By turning off lots of transistors at once, stacking the semiconductor device lowers the subthreshold leakage current [13].

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Journal of Futuristic Sciences and Applications, Volume 4, Issue 2, Jul-Dec 2021
Doi: 10.51976/jfsa.422105

Figure 1: Sleep Transistor Technique

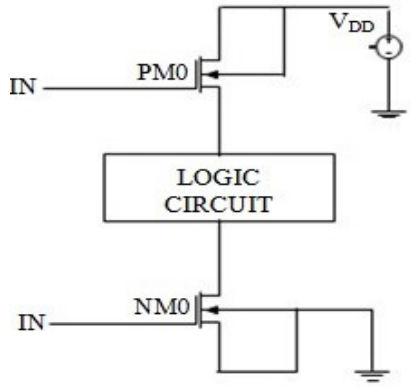
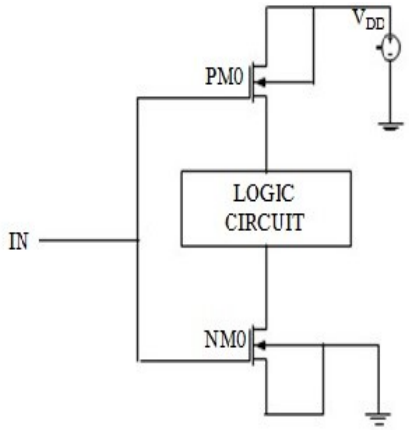


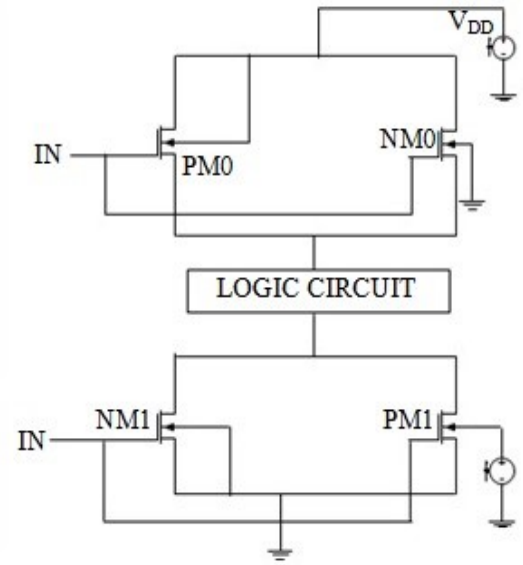
Figure 2: Forced Stack Technique



1.1.3 Dual sleep technique

Every component in the circuit is either NMOS or NMOS-like (NM0 and NM1). On the other hand, the header and footer employ NMOS and PMOS transistors, respectively. The two options are "on" and "off" [14]. These two devices operate normally when not used, as seen in Figure 3.

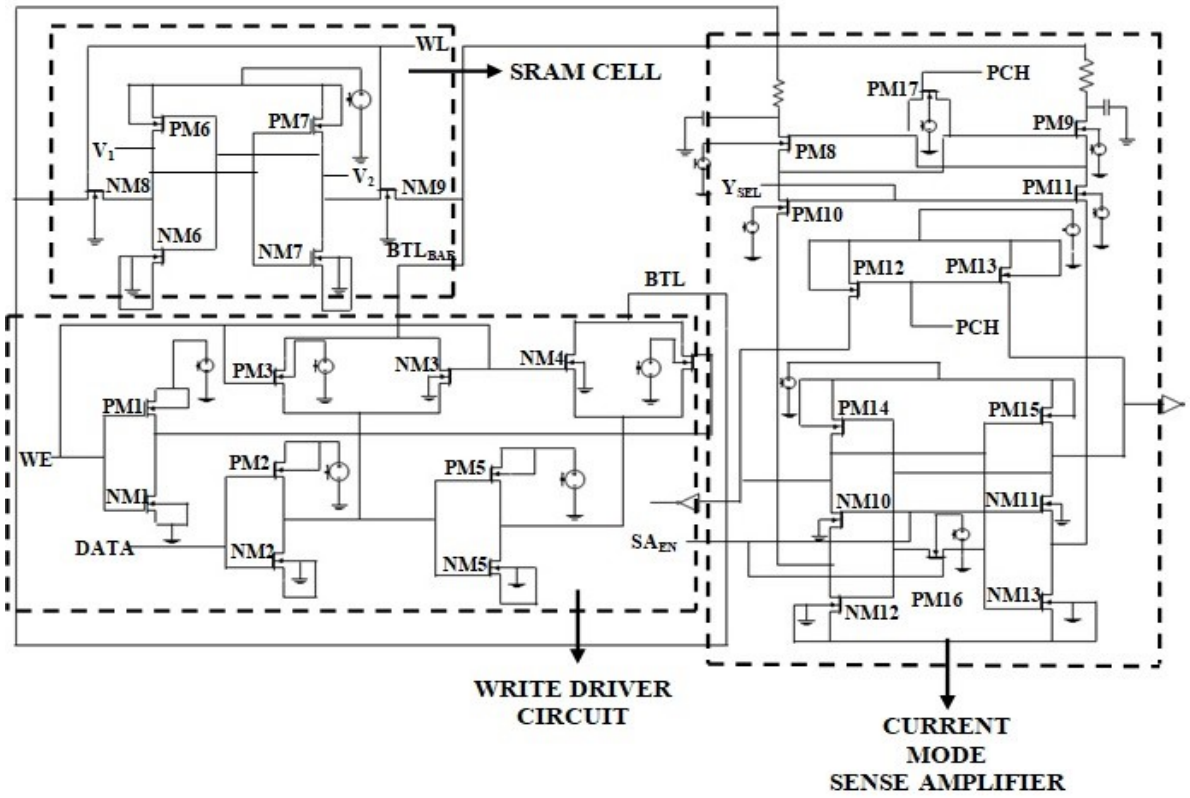
Figure 3: Dual Sleep Technique



2.0 Single-Bit Memory Architecture

Figure 4 depicts an example of single-bit cache memory. This machine's most critical components include SRAMC/WDC/CMSA. The description has three sections: Bit, WE, and BL escape BLBAR as BLBAR moves into WDC [15,16]. The SRAMC's two output pins are designated by the letters WL and V1. Ysel/BL/BLBAR/PCH/SAEN inputs are available when the CMSA is connected to the WDC.

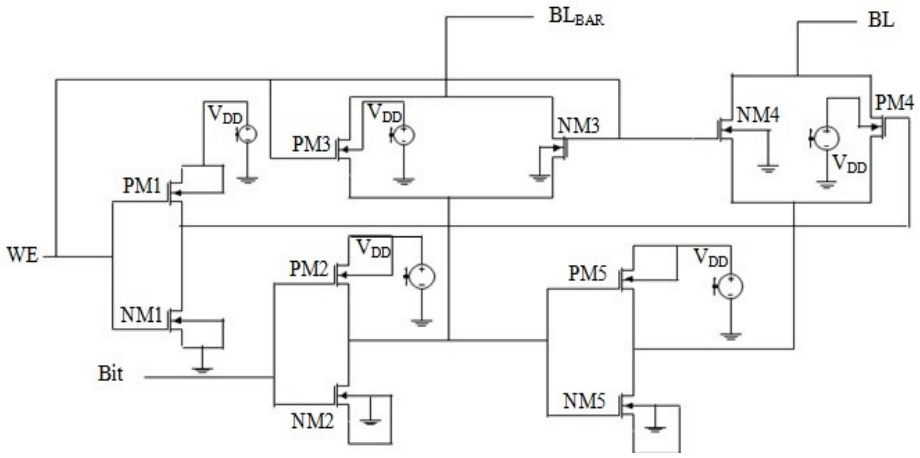
Figure 4: Single Bit Architecture



2.1 WDC

Figure 5 shows the write driver for this application. The bit line's high pre-load level is below the writing margin of the SRAMC when the WDC is turned on. With the aid of a WDC, the necessary voltage may be calculated. When WE are set to 1, all data received from an input line is sent to that line's bit lines. The word "Write Enable" is highlighted at the very top of the code. Finally, access transistors provide the data to the proper memory cell. Before the WDC, each computer bit cell was required to have a particular value [17,18].

Figure 5: WDC

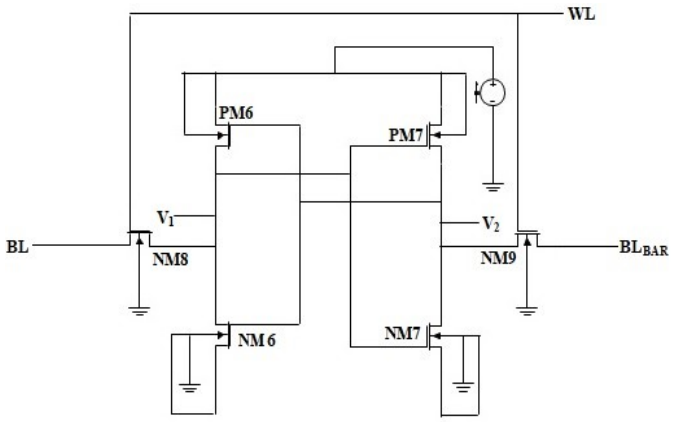


Doi: 10.51976/jfsa.422105

2.2 Conventional SRAM

The shifting of the 6T SRAMC is shown in Figure 6. Due to how much data they can store, "static RAM cells" are also known as SRAMCs. Six NM8/NM9 NMOS transistors and six CMOS inverters serve as access transistors for the SRAMC (PM6, PM7, NM6, and NM7). The cross-coupled inverters for each bit are constructed using transistors and SRAMC. The only possible values in the cell [19,20] are 0 or 1. In a bi-stable latching circuit, two inverters control six SRAMC transistors.

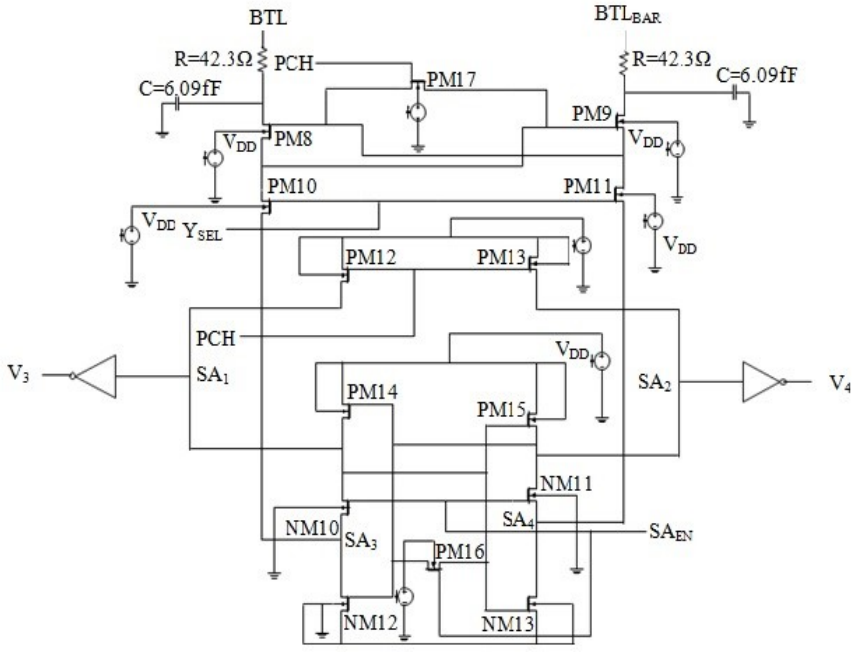
Figure 6: Conventional SRAM



2.3 CTDSA

The sensing amplifier plays a key role in the cache memory's construction. Only one of the two-bit lines is wired to the power source during reading. A current sense amplifier comprises various parts that talk to one another [21-23].

Figure 7: CTDSA



3.0 Analysis of Result

In this section, the output of each circuit is described and rated. Figure 8 displays the SAEN, WL, and CMSA open and reading data. This sensing amplifier can read only the bit lines of SRAM cells. The bit lines provide data to V3 and V4.

Figure 10: CTDSA Output Waveform

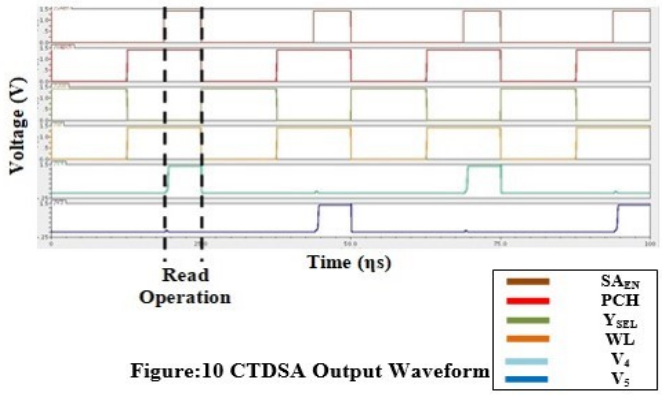


Figure:10 CTDSA Output Waveform

Table 1: SBSCMSA Different Parameter

S.No.	Parameters	Power Consumption	Sensing Delay
1.	R=42.3Ω	25.78μW	20.41ηs
2.	R=42.3KΩ	30.87μW	20.41ηs

Less power is needed as the resistance rises. A circuit's resistance impacts its size, functionality, and speed. In essence, it makes the spread of authority more challenging.

Table: 2 Different Parameters While Utilizing Different Power-Reduction Methods Over SA

Techniques \ Architecture	SBSCMSA		
	Power Consumption	**Sensing Delay**	**No. of Transistors**
Dual Sleep	26.68 μW	20.11 ηs	40
Sleep Transistor	26.78 μW	20.51 ηs	38
Forced Stack	26.88 μW	20.81 ηs	38

To cut down on power usage when using a forced stack technique, CMSA uses the SRAM strategy shown in Table 3.

Table 3: Utilizing Various Power Reduction Techniques, SRAM with CMSA Power Consumption

Technqiues	SBSCMSA	
	Power Consumption	**Sensing Delay**
Dual Sleep	24.32 μW	20.11 ηs
Sleep Transistor	26.55 μW	20.51 ηs
Forced Stack	25.55 μW	20.81 ηs

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4.0 Conclusion

Researchers examined single-bit cache memory to determine its effectiveness. Single-bit cache memory comprises a write driver circuit, a static random access memory cell, and a current mode detection amplifier. Single-bit cache memories can consume less power using sleep transistors, forced stacks, and dual sleep on components like current-mode sensors and static random-access memories. In this study, it was discovered that SRAM cells consumed less power than single-bit caches.

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