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Analysis of Cache Memory Architecture Design Using Microprocessor Low Power Reduction Techniques

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ABSTRACT

The single-bit cache memory architecture is investigated in this paper. An SRAM cell, a write driver circuit, and a current latch detector amplifier make up a single-bit cache. The architecture's transistor count, power usage, sensing delay, and other aspects are evaluated using various resistance settings. R must be at its ideal value to compare and use the forced stack, dual sleep, and sleep transistor approaches. The least amount of power is used when SRAM cells are stacked using CLSA. Monte Carlo simulations were used to evaluate the circuit's reliability. Using Cadence Virtuoso, all 45-ηm CMOS technologies were simulated.

Keywords: *Current Latch Sense Amplifier (CLSA); Write Driver Circuit (WDC); Static Random-Access Memory Cell (SRAMC); Sense Amplifier (SA).*

1.0 Introduction

Wireless sensor networks have significantly changed how we go about our daily lives. One of the many applications for sensor networks is using sensors to monitor the environment. These gadgets have a wide range of applications, including surveillance in the military and medical diagnosis. A collection of wireless sensors called the body area network (BAN) can be used to identify health problems. Body area networks must constantly monitor their patients' vital signs to deliver timely information. With body area networks, physiological markers can be continuously monitored. Continuous environmental monitoring produces better results than brief hospital stays. The body area network can function better since fewer wireless sensor nodes can be trusted. The sensor nodes must be as small as possible to avoid obstructing eyesight. The amount of energy the sensor can store depends on the size of the batteries. According to Malan [1-2], medical wireless sensor nodes' unpleasant design makes it challenging to replace the batteries in these devices.

1.1 Power reduction techniques

The circuit's performance and speed can be improved without compromising power consumption.

1.1.1 Sleep transistor technique

State-destructive techniques damage the transistors when connected to the power source of a sleep transistor or ground. These operating modes are referred to as gated-GND and VDD. Those looking to connect with others might find a list of people more interested in technology here [3]. To

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save power, the logic circuits disable the sleep transistor when the system is in "standby" mode. Sleeping semiconductor technology can drastically reduce sleep power by removing sleep transistors from logic networks, as demonstrated in Figure 1. (a).

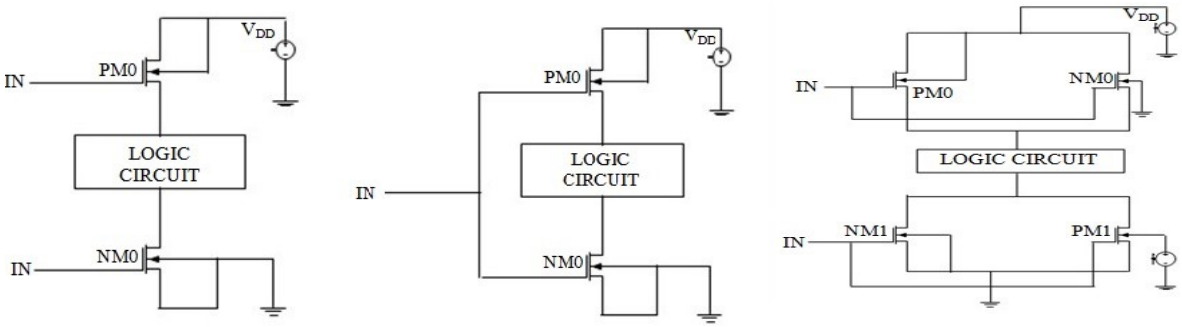
1.1.2 Forced stack technique

Figure 1(b) illustrates forced stacking. As an alternative, transistors can be stacked to use less energy. Transistor stacking reduces leakage current by simultaneously turning off every transistor [4].

1.1.3 Dual sleep technique

MOS transistors contain PM0 and PM1, while CMOS transistors contain PM1 and PM2 (NM0 and NM1). The header and footer transistors on the page are each NMOS and PMOS transistors. A transistor that is both on and off is said to be on. Figure 1 (c) shows the standby mode using NMOS and PMOS transistors. This tactic has been used to limit the quantity of energy we consume [5].

Figure 1: (a) Sleep Transistor Technique; (b) Forced Stack Technique; (c) Dual Sleep Technique



2.0 Single-Bit Memory Architecture

Figure 2: Schematic of Single Bit Cache Memory Architecture

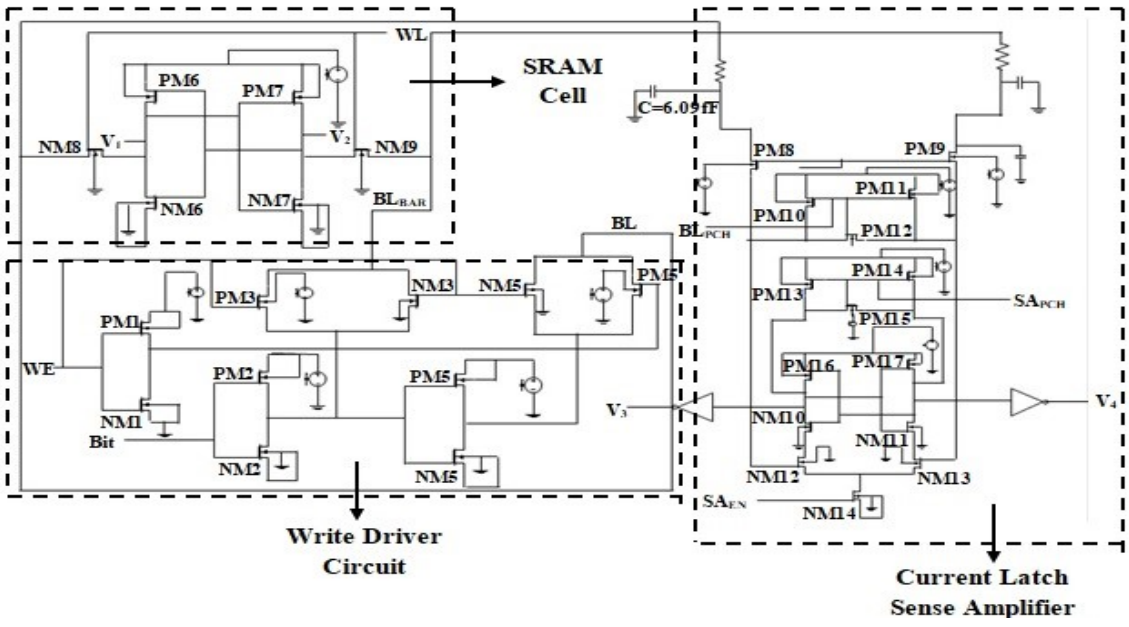
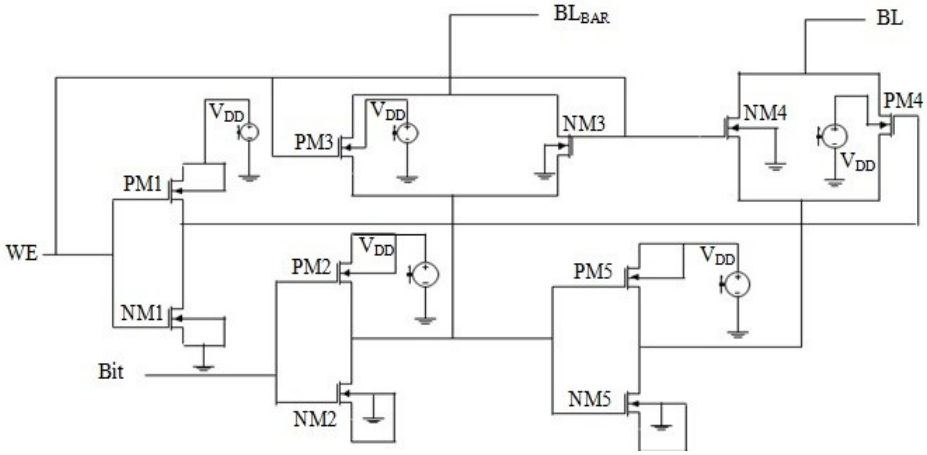


Figure 2 depicts the single-bit cache memory architecture comprising WDC, SRAMC, and CLSA blocks. The WDC's input pins allow for feeding both bits and words (WE). Additionally, there are two types of output connectors (BL and BLBAR). The bit lines (BL and BLBAR), the word line (WL), and the SRAMC are all coupled (V1 and V2). Four input pins and two output pins make up CLSA.

2.1 WDC

Users can write on the device thanks to the driver schematic (Figure 3). For the WDC to function, pre-load levels on a bit line must be lower than the writing margin of the SRAMC [6-9]. When delivering data to a particular memory cell, the "WE=1" command instructs the WDC Access transistors how much voltage to apply to the bit line to create the desired value (write enable pulled high). As a result, the buffer is placed before the WDC output. The bit cell must have a specific value before the WDC may receive it. For the circuit to write the desired bit, the bit lines of the memory cell must first be charged and then discharged [10-14].

Figure 3: WDC Schematic



2.2 Conventional SRAM

Figure 4: SRAM Cell Schematic

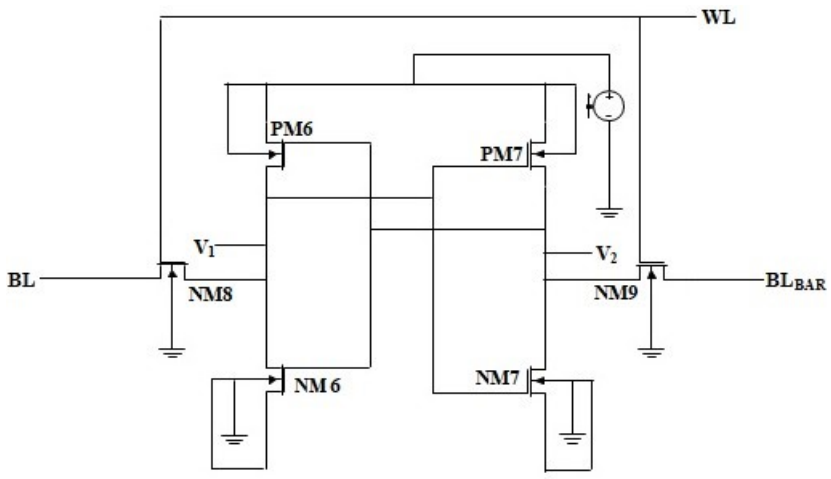


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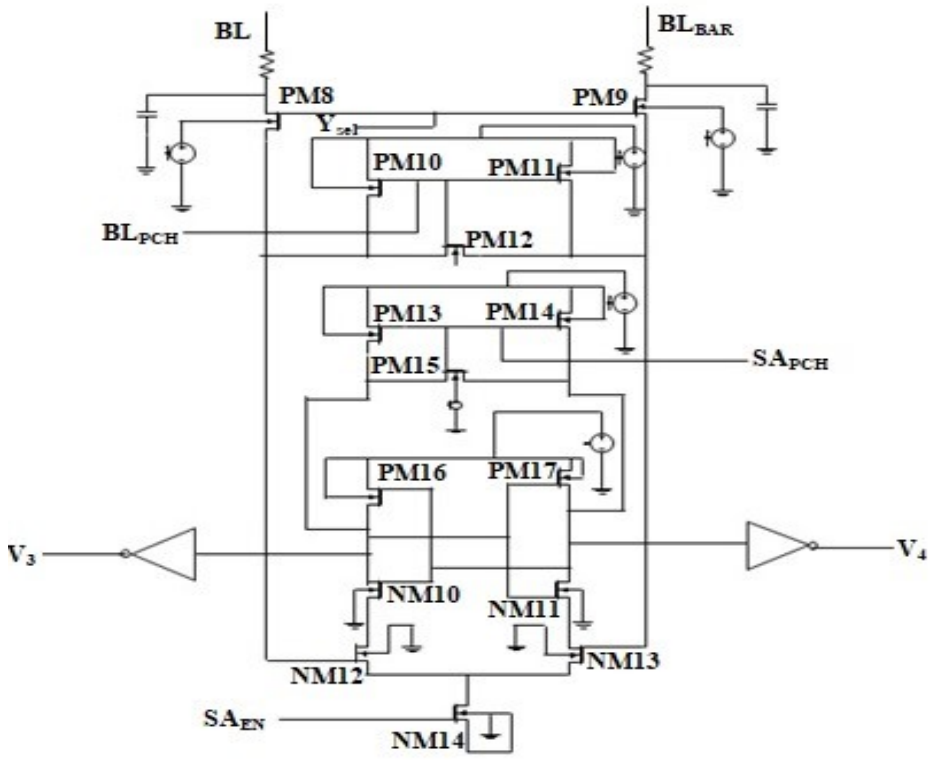
Figure 4 depicts the 6T SRAMC schematically. Static RAM Cell is the name given to a device with a huge storage capacity. The SRAMC contains six transistors, four PMOS transistors, two NM8/9 access transistors, and two CMOS inverters (PM6, PM7, NM6, and NM7). The SRAMC and transistors produce two cross-coupled inverters for each bit. This cell has only two possible values: 0 and 1 [15, 16].

2.3 CLSA

The employment of the sensing amplifier changes the cache memory's physical composition. Part of the supply voltage is sent to the one-bit line while the other bit line is drained. A sufficient bit line capacity is necessary to ensure that transistors can be accessed quickly and that bit cells don't drain too slowly. As a result, saturation magnifies slight variations in bit line voltages [17, 18]. Figure 5 shows the circuit schematic for a current latch sensing amplifier.

Figure 5: CLSA Schematic



Bit lines transmit the changes between SA3 and SA4 CLSA input voltages. When SA1 and SA2 start to discharge their charge quickly, SAEN rises [19,20]. These components work together to increase the potency of NM12 over NM13. As a result, the output V3 can have a lower power loss than the output V4.

3.0 Analysis of Result

The output of the WDC is shown in Figure 6 for the following situations: While VDD is the BL, VDD/2 is the BLBAR. If Bit and WE are both 0V, then BL and BLBAR are both VDD/2.

Figure 6: WDC Output Waveform

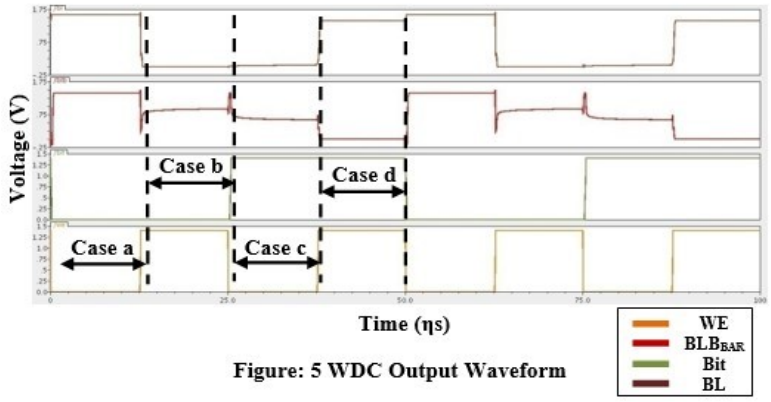


Figure: 5 WDC Output Waveform

The writing and holding operations for SRAM cells are shown in Figure 7. The sensing amplifier stores and retrieves data using transistors, NM6 and PM6 (NM8 and NM9). For reading and passing SRAM cell bit lines, the sensing amplifier only has access to V3 and V4. Figure 8 shows what happens when SAEN and WL are active in CLSA.

Figure 7: STSRAM Cell Output Waveform

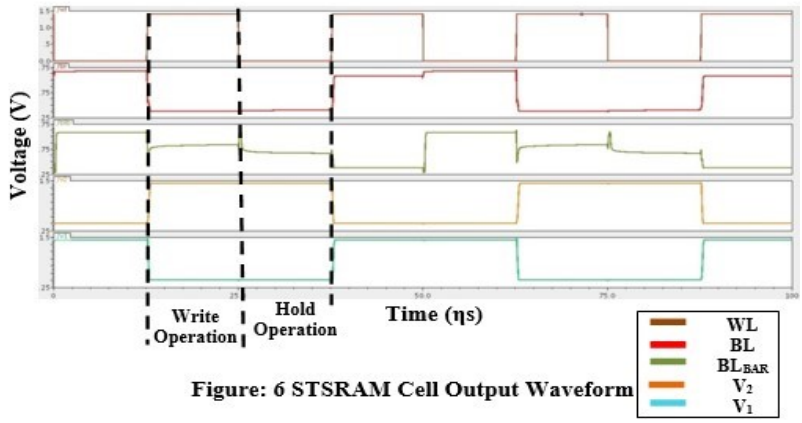


Figure: 6 STSRAM Cell Output Waveform

Figure 8: Current Latch Sense Amplifier Output Waveform

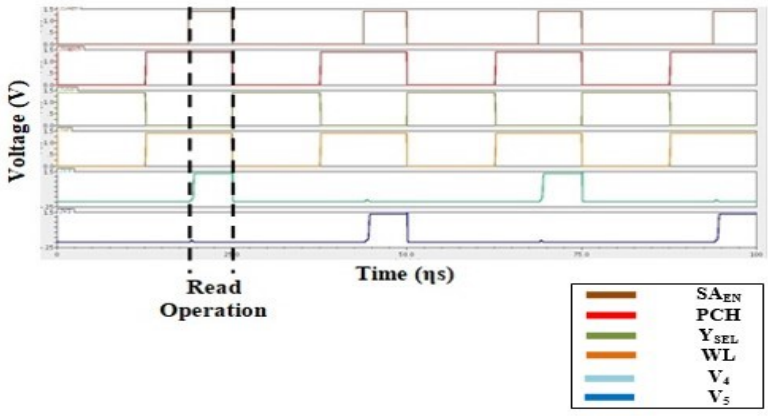


Figure: 9 Current Latch Sense Amplifier Output Waveform

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Table: 1 Variable in Single-Bit Cache Memory Architecture

S.No.	Parameters	Power Consumption	No. of Transistors	Sensing Delay
1.	R=42.3Ω	82.83μW	36	29.92ηs
2.	R=42.3KΩ	30.51μW	36	29.92ηs

Table 2: Single Bit Cache Memory Architecture Power Consumption with Power Saving Methods Applied Over CLSA

S.No.	Techniques	Total Power Consumption	Sensing Delay	No. of Transistors
1.	**Sleep Transistor Technique**	32.10μW	30.25ηs	38
2.	**Forced Stack Technique**	23.5μW	30.76ηs	38
3.	**Dual Sleep Technique**	30.01μW	30.12ηs	40

CLSA can save more energy when a circuit's resistance rises while using less power. For CLSA and SRAM cells, methods for reducing power consumption are displayed in Table 3. The most energy-efficient design for a single-bit cache memory is forced stack, not SRAM or CLSA. Electricity use and taking up space are mutually exclusive.

Table 3: Power Consumption of Single Bit Cache Memory Architecture Using SRAM Cell and CLSA Power Reduction Techniques

S.No.	Techniques	Total Power Consumption	Sensing Delay	No. of Transistor
1.	**Sleep Transistor Technique**	30.12μW	20.85ηs	40
2.	**Forced Stack Technique**	20.51μW	20.92ηs	40
3.	**Dual Sleep Technique**	30.14μW	19.12ηs	44

4.0 Conclusion

Single-bit cache memory is produced using a WDC, an SRAM cell, and a current latch detecting amplifier. On single-bit cache memory, various levels of resistance have also been tried. CLSA and SRAM cells use a sleep transistor technique to save energy. The forced stack and dual seeps are a couple of more methods. Power consumption decreases as R grows for CLSA cache memory systems and SRAM cells using forced stacking techniques. Additionally, Monte Carlo and process corner simulation have been used to examine this kind of task is better completed at a separate time.

References

1. Y. He, J. Zhang, X. Wu, X. Si, S. Zhen, and B. Zhang, "A Half-Select Disturb-Free 11T SRAM Cell With Built-In Write/Read-Assist Scheme for Ultralow-Voltage Operations," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 10, pp. 2344-2353, Oct. 2019, doi: 10.1109/TVLSI.2019.2919104.

2. R. Fragasse et al., "Analysis of SRAM Enhancements Through Sense Amplifier Capacitive Offset Correction and Replica Self-Timing," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 6, pp. 2037-2050, June 2019, doi: 10.1109/TCSI.2019.2902102.

3. Tripathi Tripti, Chauhan D. S., Singh S. K., and Singh S. V. "Implementation of Low-Power 6T SRAM Cell Using MTCMOS Technique", In Advances in Computer and Computational Sciences, Springer, Singapore, 2017.

4. 4.M.Geetha Priya, Dr.K.Baskaran, D.Krishnaveni. "Leakage Power Reduction Techniques in Deep Submicron Technologies for VLSI Applications." ELSEVIER, International Conference on Communication Technology and System Design 2011.

5. K Sridhara, G S Biradar, Raju Yanamshetti, "Subthreshold leakage power reduction in VLSI circuits: A survey," Communication and Signal Processing (ICCSP) 2016 International Conference on, pp. 1120-1124, 2016.

6. S. Gupta, K. Gupta, B. H. Calhoun, and N. Pandey, "Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 978-988, March 2019, doi: 10.1109/TCSI.2018.2876785

7. H. Dounavi, Y. Sfikas, and Y. Tsiatouhas, "Periodic Aging Monitoring in SRAM Sense Amplifiers," 2018 IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS), Platja d'Aro, 2018, pp. 12-16, doi: 10.1109/IOLTS.2018.8474169.

8. S. Ahmad, B. Iqbal, N. Alam, and M. Hasan, "Low Leakage Fully Half-Select-Free Robust SRAM Cells With BTI Reliability Analysis," in IEEE Transactions on Device and Materials Reliability, vol. 18, no. 3, pp. 337-349, Sept. 2018, doi: 10.1109/TDMR.2018.2839612

9. B. N. K. Reddy, K. Sarangam, T. Veeraiah, and R. Cheruku, "SRAM cell with better read and write stability with Minimum area," TENCON 2019 - 2019 IEEE Region 10 Conference (TENCON), Kochi, India, 2019, pp. 2164-2167, doi: 10.1109/TENCON.2019.8929593.

10. A. Surkar and V. Agarwal, "Delay and Power Analysis of Current and Voltage Sense Amplifiers for SRAM at 180nm Technology," 2019 3rd International Conference on Electronics, Communication, and Aerospace Technology (ICECA), Coimbatore, India, 2019, pp. 1371-1376, doi: 10.1109/ICECA.2019.8822122.

11. Gomes Iuri A.C., Meinhardt Cristina, Butzen Paulo F. "Design of 16nm SRAM Architecture" South Symposium on Microelectronics, 2012.

12. Chakka Sri Harsha Kaushik, Rajiv Reddy Vanjarlapati, Varada Murali Krishna, Tadavarthi Gautam, V Elamaran, "VLSI design of low power SRAM architectures for FPGAs," Green Computing Communication and Electrical Engineering (ICGCCEE) 2014 International Conference on, pp. 1-4, 2014.

Doi: 10.51976/jfsa.322003

13. Richa Choudhary, Srinivasa Padhy, Nirmal Kumar Rout, "Enhanced Robust Architecture of Single Bit SRAM Cell using Drowsy Cache and Super cut-off CMOS Concept," International Journal of Industrial Electronics and Electrical Engineering, Volume-3, PP.63-68, July 2011.

14. Jesal P. Gajjar, Aesha S. Zala, Sandeep K. Aggarwal, "Design and Analysis of 32 bit SRAM architecture in 90nm CMOS Technology" Volume: 03, Issue: 04, Apr-2016, pp:2729-2733.

15. Reeya Agrawal, V. K. Tomar. "Analysis of Cache (SRAM) Memory for Core I ™ 7 Processor",9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), 2018,402.

16. Kundan Vanama, Rithwik Gunnuthula, Govind Prasad, "Design of low power stable SRAM cell," Circuit Power and Computing Technologies (ICCPCT) 2014 International Conference on, pp. 1263-1267, 2014.

17. Rakesh Dayaramji Chandankhede, Debiprasad Priyabrata Acharya, Pradip Kumar Patra, "Design of High-Speed sense Amplifier for SRAM," IEEE International Conference on Advanced Communication Control and Computing Technologies, pp. 340-343.

18. Zikui Wei, Xiaohong Peng, JinhuiWang, Haibin Yin, Na Gong, "Novel CMOS SRAM Voltage Latched Sense Amplifiers Design Based on 65nm Technology" pp.3281-3282.

19. Baker Mohammad, Percy Dadabhoy, Ken Lin, Paul Bassett. "Comparative study of current mode and voltage mode sense amplifier used for 28nm SRAM." 24th International Conference on Microelectronic, 07 March 2013

20. Manoj Sinha, Steven Hsu, Atila Alvandpour, Wayne Burleson, Ram Krishnamurthy, Shekhar Borhr. "High-Performance and Low-Voltage Sense-Amplifier Techniques for sub-90nm SRAM." SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip].