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Performance Analysis of LNA for IoT Application using Noise Cancellation Technique

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ABSTRACT

Using a noise amplifier cancellation approach, a quantitative and yield test on a low-noise amplifier was completed. A single inductor on a common source line can be used to construct a device with a broad bandwidth, low noise figures (NF), and high-power gain. The suggested low-noise amplifier uses complementary metal-oxide semiconductor technology for the optimum power gain and noise figure.

Keywords: *Complementary Metal Oxide Semiconductor (CMOS); Low Noise Amplifier (LNA); Common Source (CS); Common Gate (CG).*

1.0 Introduction

Mobile sensor networks are an intriguing notion for scientists (WSNs). They work in various fields, including environmental safety, process control, and field monitoring. WSNs are challenging to install because of their low cost, strong interoperability, and low power consumption. These networks depend heavily on battery power. The receivers must use less power and receive signals more clearly if they are to last longer [1-3]. Figure 1 depicts the basic WSN. CMOS technology is a great option for WSNs because of its modest capacity, low cost, and strong interoperability with other technologies [4–9]. Both analog and radio frequency technologies are used in these systems. The LNA is crucial because it serves as the initial RF receiver in WSN [10–14]. This device is made to lessen background noise, primarily produced by antenna RF emissions. Efficiency, linearity, impedance, and power consumption should all be considered. LNA architectures are typically designed using CS and CG topologies [15–20].

The first part of the receiver's front end is an amplifier with little noise (LNA). At [21-31], the first block of amplification starts. Only at a voltage of 1 Vp can the antenna's signal be picked up because it is so weak. In the initial step, the LNA amplifies the antenna's weak signal. The best module design is essential when the market for wireless networks is big. The quantity and caliber of the noise in the receiver circuit are directly correlated. As a result, we can receive a noise-free signal with value for information. The LNA's topology is incredibly straightforward. In industrial architecture, a single-chip component and an NMOS transistor are integrated. As a result, equipment is more dependable and less expensive. In the MOS VLSI technique, the scaling canal's length was cut by nanometres, and the passage rate was increased by gigahertz [32,33].

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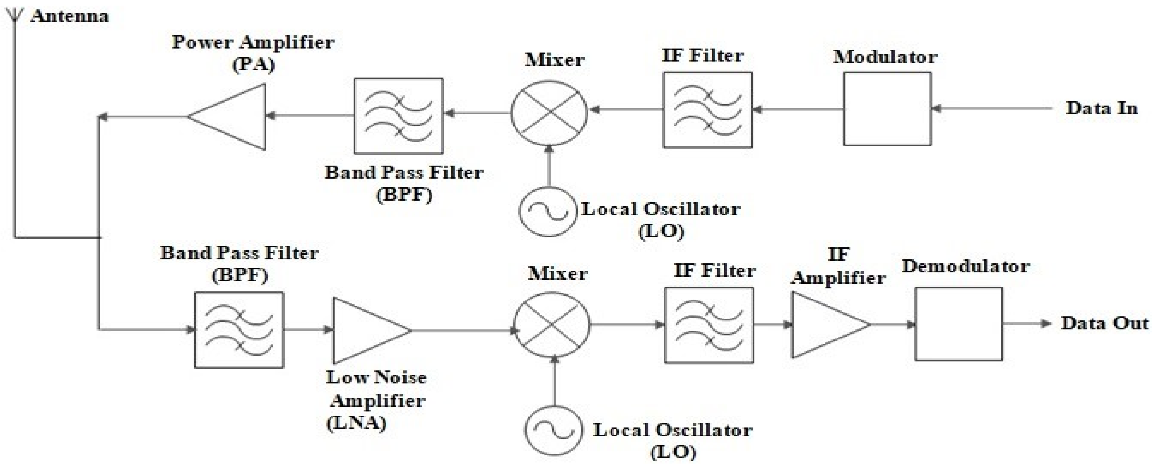
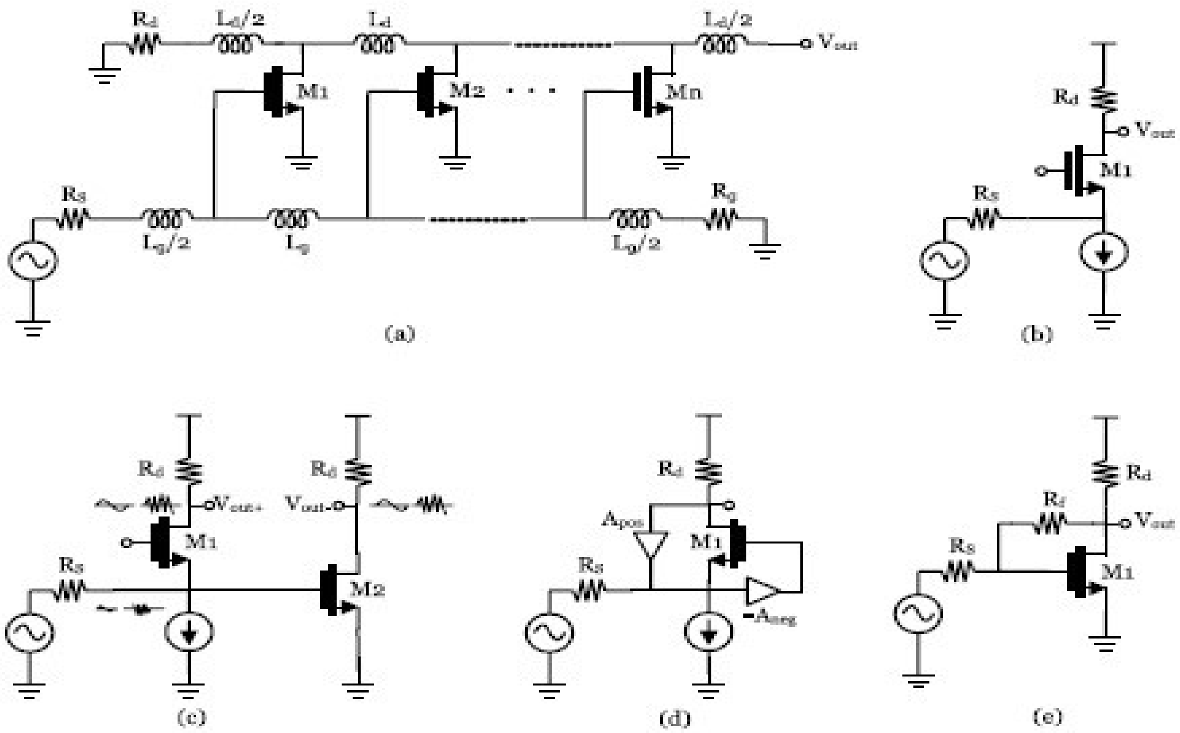
Figure 1: LNA Basic Block Diagram



Distributed amplifiers can be employed to cover a significant portion of the multi-gigahertz spectrum while preserving high bandwidth, as shown in Figure 2. (a). The distributed amplifier requires numerous stages and inducers, which uses up a lot of chip space and power. Additionally, the CG transistor is used. A CG transistor's input impedance is 1 / gm, where gm is the transistor's transduction. With the Gm 20 ms arrangement, this 50-input wideband match has two major wideband matching problems [7–9]. The coefficient of thermally acoustic noise, which determines thermally acoustic noise (NF), is fixed to the input criterion and cannot be increased or decreased to reduce NF and raise power consumption. The performance of the CG stage circuit can be enhanced by feedback and noise. Figure 2 illustrates how LNA noise can be eliminated.

Figure 2: Architectures of Wideband LNA



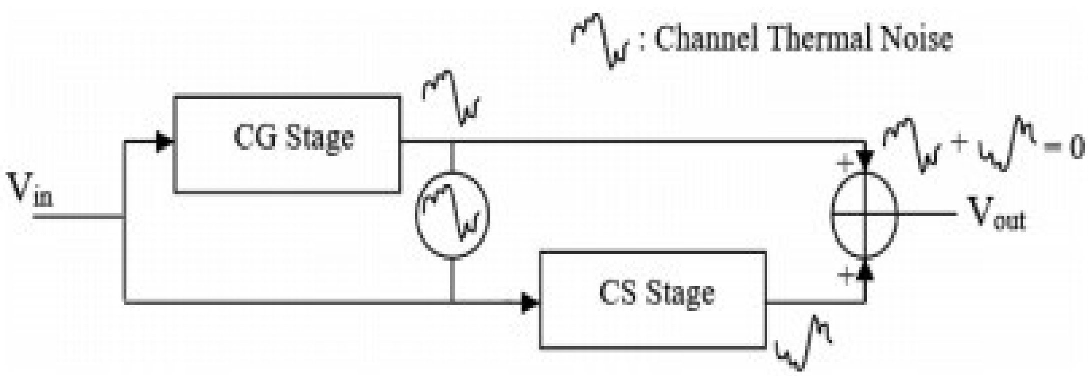
Techniques to reduce background noise have been demonstrated to improve NF. However, these methods need more energy because of the intermediate processes and high voltage supply. Figure 2 shows how input and feedback were applied to separate the NF, identify and match parasite entry locations, increase parasite power, and restrict operational bandwidths (d). In these situations, it isn't easy to create a comprehensive, low-energy plan using CG input. Utilizing a resistive feedback architecture can be advantageous for creating a wideband LNA. A 50-input needs to have a feedback resistor attached to it to operate for wideband, as shown in Fig. 2. (e). It covers a larger range of frequencies and is more effective and quieter than other circuits.

2.0 Analysis of Design

The CG amplifier is more sensitive to high voltage and has headroom concerns in inductor-free LNA than in CS architecture because the RF signal flow in the field must be divided by some means. The main source of amplification in this configuration is a CS amplifier. For example, as seen in Figure 2, (a). However, the performance of the NF amplifier will be adversely affected by passive resistors or active components. To achieve an acceptable noise efficiency for an inductor-free LNA with CS architecture, a 50-input matching network that produces no or very little noise is required [34]. CG Topology may be used to change the input impedance, which makes it handy for matching inputs. Noise cancellation technology is included in CG amplifiers to lessen the amount of noise they produce. A CS amplifier can also build a low-noise inductive network [35–39].

A hypothetical system with two behavior amplifiers that can be used to study structure is depicted in Figure 3. Signals from two separate sources can be combined using an adder [40–44].

Figure 3: LNA Structure



3.0 LNA Proposed Design

Cs amplifiers, one of the three fundamental voltage or transconductance amplifiers, are constructed mostly using field-effect transistors (FET). The port is where the signal is sent, and the drain is located here. There is a further terminal designated as "normal." One computer is connected to the mainframe to keep things straightforward [45–49].

A CG path of M4, R2, and DC source I1 is created when four CG amplifiers are connected, as shown in Figure 1. M1 transduction regulates a third to a half of the circuit's overall input impedance (gm1). Figure 4 illustrates how Gm1 was selected to fit an RG.

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Figure 4: Diagram of LNA using Noise Cancellation Technique

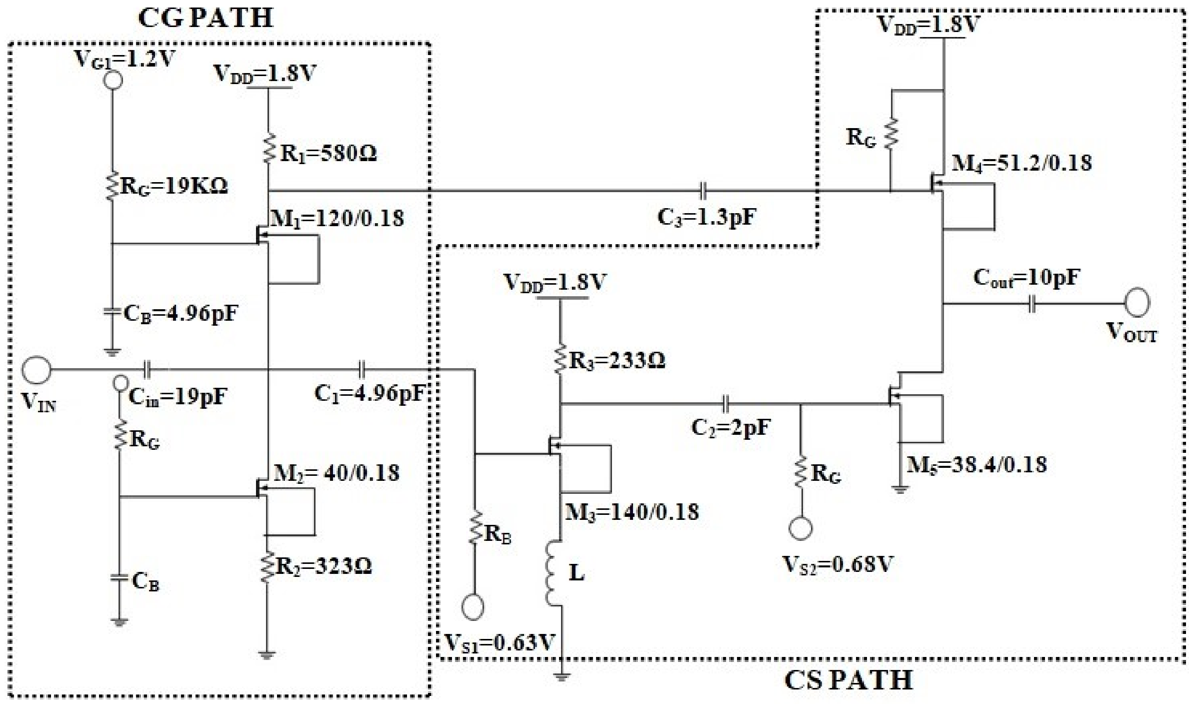

Figure 5 depicts two types of adders that can handle sounds and signals from various angles. Type1 adders have two branches for typical load, but Type2 adders only have one [55–59].

The MT1 and MT2 trans conductor cables can be changed, and the Type 1 extension allows you to change the voltage gain ratio between active routes. Utilizing energy is a factor in the equation as well. Due to their smaller size, Type2 adder machines typically produce more noise than Type1 adder machines. This suggests that employing MO1 can lessen the noise produced by Type 2 MO2. Then, Type2 was added to this design as a second notion. The second stage of the CS amplifier again uses the Type 2 adder.

Figure 5: Adder Type

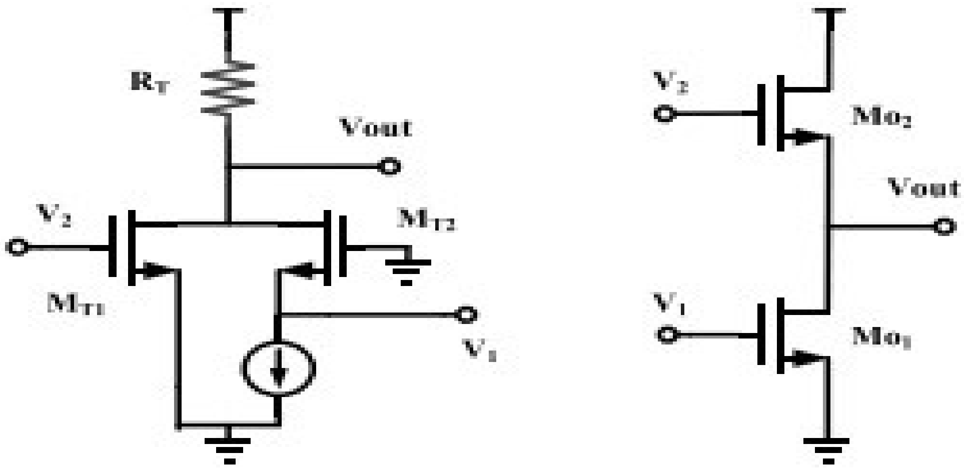

Figure 6: Small-Signal Diagram of LNA

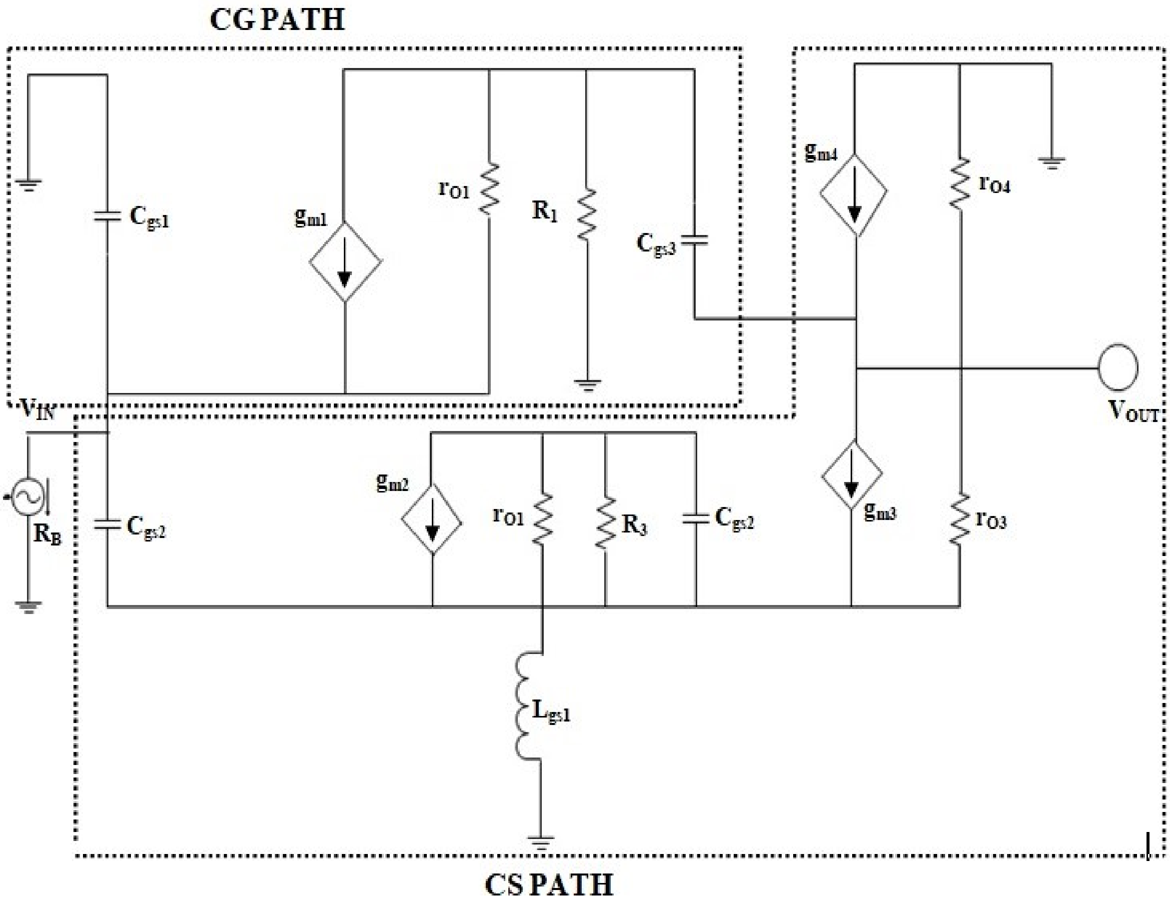

Figure:7 S11 value indicates that the reflection coefficient should be less than zero. Figure 8 depicts the suggested LNA's S21 parameter.

Figure 7: Shows the S_{11} Parameter of Design

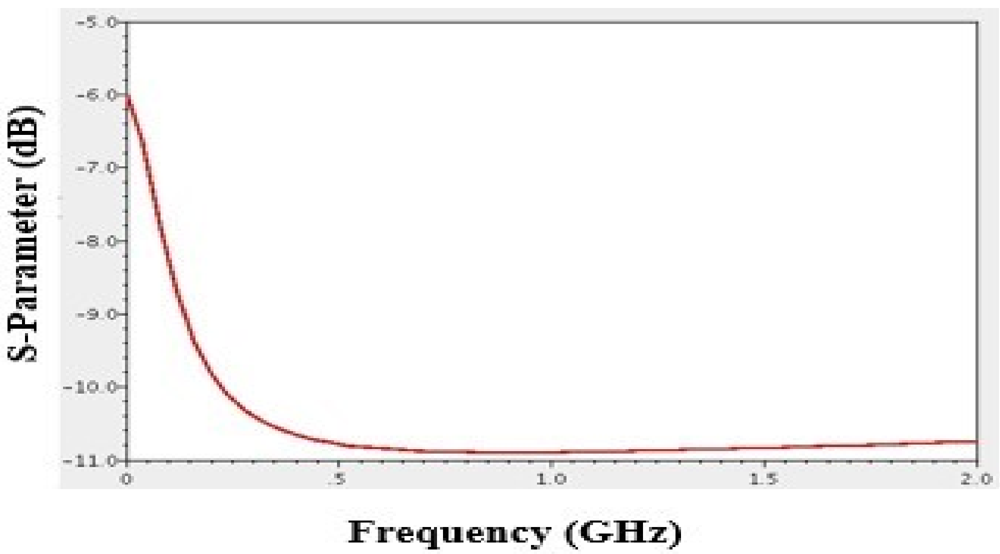

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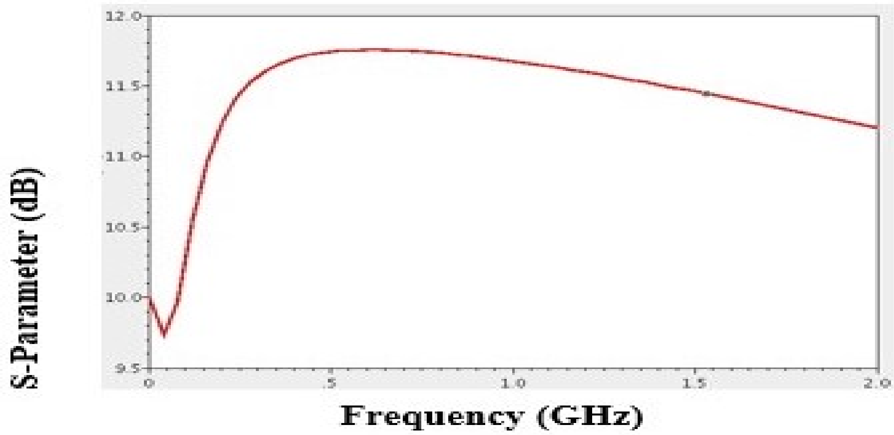
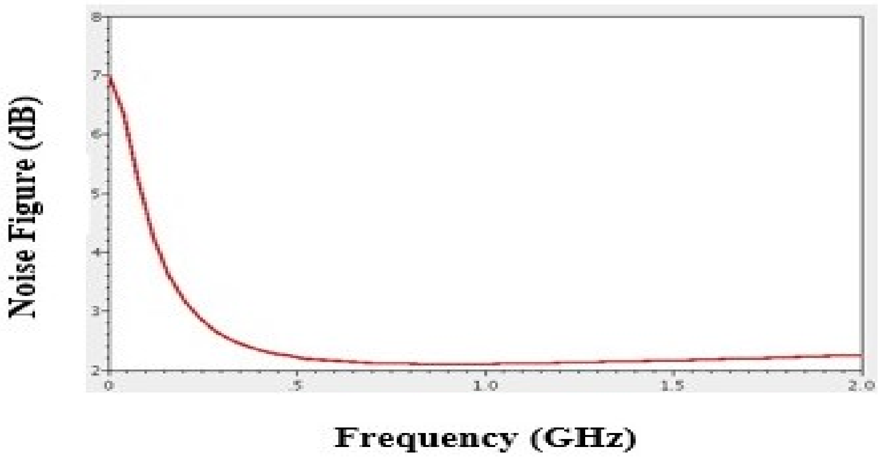
Figure 8: Shows the S_{21} parameter of Design



Based on the architecture, nearly identical noise statistics are presented in Figure 9.

Figure 9: Shows Noise Figure Design



4.0 Conclusion

The noise amplifier cancellation method of a high sensitivity receiver was used to assess and compare the yield of low noise amplifiers. A low noise figure (NF) and a single inductor connect a high-power gain, the CS path, and the CG path to provide a broad bandwidth. Packaging the LNA in UMC 90um CMOS technology with a 1.2V supply allows for a maximum power gain of 20.5dB and an NF of 2-2.5dB.

References

1. N. Yadav, A. Pandey, and V. Nath, "Design of CMOS low noise amplifier for 1.57GHz," 2016 International Conference on Microelectronics, Computing and Communications (MicroCom), Durgapur, 2016, pp. 1-5.

2. J. Kim and J. Silva-Martinez, "Low-power, low-cost CMOS direct-conversion front-end for multistandard applications," IEEE J. Solid-State Circuits, vol. 48, no. 9, pp. 2090–2103, Sep. 2013.

3. M.-T. Lai and H.-W. Tsao, "Ultra-low-power cascaded CMOS LNA with positive feedback and bias optimization," IEEE Trans. Microw. Theory Techn., vol. 61, no. 5, pp. 1934–1945, May 2013.

4. F. Belmas, F. Hameau, and J.-M. Fournier, "A low power inductors LNA with double Gm enhancement in 130 nm CMOS," IEEE J. SolidState Circuits, vol. 47, no. 5, pp. 1094–1103, May 2012.

5. E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari, E. Sanchez-Silencio, "A 2.8-mW sub-2-dB noise-figure inductor less wideband CMOS LNA employing multiple feedback," IEEE Trans. Microw. Theory Techn., vol. 59, no. 12, pp. 3154–3161, Dec. 2011.
6. M. Parvizi, K. Allidina, and M. N. El-Gamal, "An ultra-low-power wideband inductor less CMOS LNA with tunable active shunt-feedback," IEEE Trans. Microw. Theory Techn., vol. 64, no. 6, pp. 1843–1853, Jun. 2016.

7. F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," IEEE J. SolidState Circuits, vol. 39, no. 2, pp. 275–282, Feb. 2004.

8. W.-H. Chen, G. Liu, B. Zdravko, and M. A. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," IEEE J. Solid-State Circuits, vol. 43, no. 5, pp. 1164–1176, May 2008.

9. S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling, and distortion-canceling," IEEE J. Solid-State Circuits, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

10. J. Shim, T. Yang, and J. Jeong, "Design of low power CMOS ultra-wideband low noise amplifier using the noise-canceling technique," Microelectron. J., vol. 44, no. 9, pp. 821–826, Sep. 2013.

11. K.-H. Chen and S.-I. Liu, "Inductorless wideband CMOS low-noise amplifiers using the noise-canceling technique," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 2, pp. 305–314, Feb. 2012.

12. H. Wang, L. Zhang, and Z. Yu, "A wideband inductor less LNA with local feedback and noise-canceling for low-power low-voltage applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.

13. B. Razavi, "Low-noise amplifier," in RF Microelectronics, 2nd ed. Beijing, China: Publishing House of Electronics Industry, 2012, pp. 263–266.

14. T. H. Lee, "Noise," in The Design of CMOS Radio-Frequency Integrated Circuits, 2nd ed. Beijing, China: Publishing House of Electronics Industry, 2012, pp. 259–262.

15. B. Razavi, "Noise," in Design of Analog CMOS Integrated Circuits. Beijing, China: China Machine Press, 2013, pp. 212–213.

16. J. Kim, S. Hoyos, and J. Silva-Martinez, "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization," IEEE Trans. Microw. Theory Techn., vol. 58, no. 9, pp. 2340–2351, Sep. 2010.

17. J. Kim and J. Silva-Martinez, "Wideband inductor less balun-LNA employing feedback for low-power low-voltage applications," IEEE Trans. Microw. Theory Techn., vol. 60, no. 9, pp. 2833–2842, Sep. 2012.

18. C. Liao and S. Liu, "A broadband noise-canceling CMOS LNA for 3.1– 10.6-GHz UWB receivers," IEEE J. Solid-State Circuits, vol. 42, no. 2, pp. 329–339, Feb. 2007.

19. J. Y.-C. Liu, J.-S. Chen, C. Hsia, P.-Y. Yin, and C.-W. Lu, "A wideband inductor less single-to-differential LNA in 0.18μm CMOS technology for digital TV receivers," IEEE Microw. Wireless Compon. Lett., vol. 24, no. 7, pp. 472–474, Jul. 2014.

20. A. L. T. Costa, H. Klimach, and S. Bampi, "A 2-decades wideband low-noise amplifier with high gain and ESD protection," in Proc. 28th Symp. Integer. Circuits Syst. Design (SBCCI), Sep. 2015, pp. 1–6.

21. S. Arshad, R. Ramzan, K. Muhammad, and Q. Wahab, "A sub-10 mW, noise-canceling, wideband LNA for UWB applications," Int. J. Electron. Commun., vol. 69, pp. 109–118, Sep. 2015.

22. H.-T. Chou, S.-W. Chen, and H.-K. Chiou, "A low-power wideband dual feedback LNA is exploiting the gate-inductive bandwidth/gain-enhancement technique.

23. Trung-Kien Nguyen, Chung-Hwan Kim, Gook-Ju Ihm, Moon-Su Yang and Sang-Gug Lee, "CMOS low-noise amplifier design optimization techniques," in IEEE Transactions on Microwave Theory and Techniques, vol. 52, no. 5, pp. 1433-1442, May 2004.

24. Srigayathri V. and M. S. Vasanthi, "Design of Low Noise Amplifier for Multiband receiver," 2016 International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET), Chennai, 2016, pp. 1603-1605.

25. P. K. Dakua, A. S. N. Varma, P. Kabisatpathy and S. Mishra, "Study on design and performance analysis of low noise high-speed amplifier," 2016 International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES), Paralakhemundi, 2016, pp. 1105-1108.

26. E. O. Farhat, K. Z. Adami, O. Casha, I. Grech, and J. G. Bij de Vacate, "Design of a wideband CMOS LNA for low-frequency band SKA application," 2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Cairo, 2015, pp. 567-571.

27. P. K. Verma and P. Jain, "A low power high gain low noise amplifier for wireless applications," 2015 Communication, Control and Intelligent Systems (CCIS), Mathura, 2015, pp. 363-367.

28. Kaamouchi ME, Smoussa M, Delatte P, Wybo G, Bens A, Raskin J-P, Vanhoenker-Janiver D (2007) A 2.4 GHz fully integrated ESD-protected low noise amplifier in 130-nm PD SOI CMOS technology. IEEE Trans Microwave Theory Tech 55:2822–2831.

29. Fatin GZ, Fatin HZ (2014) A wideband balun LNA. Int J Electron Commun (AEU) 68:653–657.

30. Hsu MT, Chang YC, Huang YZ (2013) Design of low power UWB LNA based on common source topology with current-reused technique. Microelectron J 44:1223–1230.

31. Ku KW, Huang CC (2012) A low power CMOS low noise amplifier for wireless communication 19th international conference on Microwaves, radar and wireless communications, May 21–23 Warsaw, Poland

32. Lin TH, Kaiser WJ, Pottie GJ (2004) Integrated low-power communication system design for wireless sensor networks. IEEE Commun Mag 42:142–150

33. Nguyen TK, Kim CH, Ihm GJ, Yang MS, Lee SG (2004) CMOS Low-noise amplifier design optimization techniques. IEEE Trans Microw Theory Tech 52:1433–1442.

34. Rajput SS, Jamuar SS (2002) Low voltage analog circuit design techniques. IEEE Circuits Syst Mag 2:24–42

35. Rajput SS, Jamuar SS (2002) Low voltage analog circuit design techniques. IEEE Circuits Syst Mag 2:24–42

36. Tsang TK, El-Gamal MN (2002) Gain and a frequency controllable Sub-IV 5.8 GHz CMOS LNA. ISCAS 4:795–798

37. Zhuo W, Li X, Shekhar S, Embabi SHK, Pineda de Gyvez J, Allstot DJ, Sanchez-Sinencio E (2005) A capacitor cross-coupled common-gate low-noise amplifier. IEEE Trans Circuits Syst II 52:875–879

38. Ziabakhsh S, Alavi-Rad H, Yagoub MCE (2012) A high- gain low-power 2-14 GHz ultra-wideband CMOS LNA for wireless receivers. Int J Electron Commun (AEU) 66:727–731.

39. Zokaei A, Amirabadi A (2014) A 0.13 µm dual-band common-gate LNA using active post distortion for mobile WiMAX. Microelectron J 45:921–929

Doi: 10.51976/jfsa.211907

40. A. Azizan, S. A. Z. Murad, R. C. Ismail, and M. N. M. Yasin, "A review of LNA topologies for wireless applications," 2014 2nd International Conference on Electronic Design (ICED), Penang, 2014, pp. 320-324.

41. Zhuo, W., Li, X., Shekhar, S., Embabi, S. H. K., et al. (2005). A capacitor cross-coupled common-gate low-noise amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *52*, 875–879.

42. Li, X., Shekhar, S., Allstot, D. J., et al. (2005). Gm-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-μμm CMOS. *IEEE Journal of Solid-State Circuits*, *40*, 2609–2619.

43. Samavati, H., Rategh, H. R., & Lee, T. H. (2000). A 5-GHz CMOS wireless LAN receiver front end. *IEEE Journal of Solid-State Circuits*, *35*, 765–772.

44. Linten, D., Aspemyr, L., et al. (2004). Low-power 5 GHz LNA and VCO in 90 nm RF CMOS. In *IEEE Symposium on VLSI circuits* (pp. 372–375).

45. Karimi, G. R., & Nazari, E. (2010). An ultra-low-voltage amplifier design using forward body bias folded cascade topology for 5 GHz application. In *IEEE conference on industrial electronics and applications* (pp. 1838–1842).

46. Chang, C.-P., Chen, J.-H., & Wang, Y.-H. (2009). A fully integrated 5 GHz low-voltage LNA using forward body bias technology. *IEEE Microwave and Wireless Components Letters*, *19*, 176–178.

47. Kargaran, E., & Kazemi, M. M. (2010). Design 0.5V, 450μμW CMOS LNA using current reuse and forward body bias technique. In *IEEE European conference on circuits and systems for communications* (pp. 93–96)

48. Wu, D., Ru, H., et al. (2007). A 0.4-V low noise amplifier using forward body bias technology for 5 GHz application. *IEEE Microwave and Wireless Components Letters*, *43*, 543–545.

49. Lorenzo, M. A. G., & de Leon, M. T. G. (2010). Comparison of LNA topologies for WiMAX applications in a standard 90-nm CMOS process. In *IEEE conference on computer modeling and simulation* (pp. 642–647).

50. Hsieh, H.-H., Wang, J.-H., et al. (Aug. 2008). Gain-enhancement techniques for CMOS folded Cascode LNAs at low-voltage operations. *IEEE Transactions on Microwave Theory and Techniques*, *56*, 1807–1816.

51. Dehqan, A., Kargaran, E., et al. (2012). Design 0.45V,1.3mW ultra high gain CMOS LNA Using gm-boosting and forward body biasing technique. In *IEEE international midwest symposium on circuits and systems* (pp. 722–725).

52. Wang, R.-L., Chen, S.-C., Huang, C.-L., Gao, C.-X., & Lin, Y.-S. (2008). A 0.8V folded-cascade low noise amplifier for multi-band applications. In *IEEE Asia pacific on circuits and systems* (pp. 1387–1389).

53. Nguyen, T.-K., Kim, C.-H., et al. (2004). CMOS low-noise amplifier design optimization techniques. *IEEE Transactions on Microwave Theory and Techniques*, *52*, 1433–1442.

54. Li, C.-H., Liu, Y.-L., & Kuo, C.-N. (2011). A 0.6-V 0.33-mW 5.5-GHz receiver front-end using resonator coupling technique. *IEEE Transactions on Microwave Theory and Techniques*, *59*, 1629–1638

55. Hong, E.-P., Hwang, Y.-S., & Yoo, H.-J. (2007). A low-power folded RF front-end with low flicker noise for direct conversion receiver. In *IEEE conference on electron devices and solid-state circuits* (pp. 453–456).

56. Tang T., Mo, T., & Chen, D. (2011). A low-noise amplifier using subthreshold operation for GPS-L1 RF receiver. In *IEEE conference on electrical and control engineering* (pp. 4257–4260)

57. Perumana, B. G., Chakraborty, S., et al. (2005). A fully monolithic 260-W, 1-GHz subthreshold low noise amplifier. *IEEE Microwave and Wireless Components Letters*, *15*, 428–430.

58. Do, A. V., & Boon, C. C. (2008). A subthreshold low-noise amplifier optimized for ultra-low-power applications in the ISM band. *IEEE Transactions on Microwave Theory and Techniques*, *56*, PP.-286–292.

59. Wei, M.-D., Chang, S.-F., et al. (2011). A CMOS fully-differential current-reuse LNA with gm-boosting technique. In *European microwave integrated circuits conference* (pp. 378–381)

60. Walling, J. S., Shekhar, S., Allstot, D. J. (2007). A gm-boosted current-reuse LNA in 0.18um CMOS. In *IEEE radio frequency integrated circuits (RFIC) symposium* (pp. 613–616).