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IoT Applications: Analysis of MTCMOS Cache Memory Architecture in a Processor

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ABSTRACT

The main goals of the suggested inquiry are to measure how much power an amplifier uses, determine how much leaks through SRAM, and use the data. The main issue with the cache memory's design was leakage power. The charge transfer sense amplifier had the lowest value compared to other sense amplifiers' power consumption figures, even though we used MTCMOS and Footer Stack to reduce leaky power. The design included MTCMOS-CTSA and MTCMOS-SRAM memory to reduce power consumption. Fusing CTSA and SRAM with MTCMOS technology can produce low-power cache memory. This cache memory uses a lot less power than CTSA and SRAM devices

Keywords: *MTCMOS-CTSA (Charge-transfer Sense Amplifier with MTCMOS Technique); MTCMOS-SRAM (Static Random-Access Memory with MTCMOS technique); SA (Sense Amplifier); Write Driver Circuit (WDC); Precharge Circuit (PCH).*

1.0 Introduction

Energy-efficient components are necessary for today's technological society. Batteries must compensate for portable gadgets' lack of power outlets when transporting items. It makes no difference whether it is on or off; the amount of electricity it uses is decreased [1-3]. In this article, researchers will talk about a piece of technology made for the common person because it uses less energy overall. In this design, researchers chose to use MTCMOS instead of SRAM cells since Table 1 shows that leakage mitigation techniques were used on all SRAM cells. Due to this, researchers chose to use MTCMOS cells rather than SRAM cells. The least power-hungry sensing amplifiers are the VMSA, CMSA, and CTSA.

Because of this, leak-stopping methods like VMSA, CMSA, and CTSA are less efficient. The design uses MTCMOS SRAM, a WDC, PCH, VMSA, CMSA, and a CTSA. The "MTCMOS CACHE Memory Architecture" also includes WDC, MTCMOS CTSA, SRAM, and PCH. It uses, on average, 98–99 percent less energy [4] than traditional memory devices.

2.0 MTCMOS Cache Memory Architecture

2.1 WDC

In Figure 1, turning off the bit line voltage reduces the margin of the MTCMOS-write SRAM [5].

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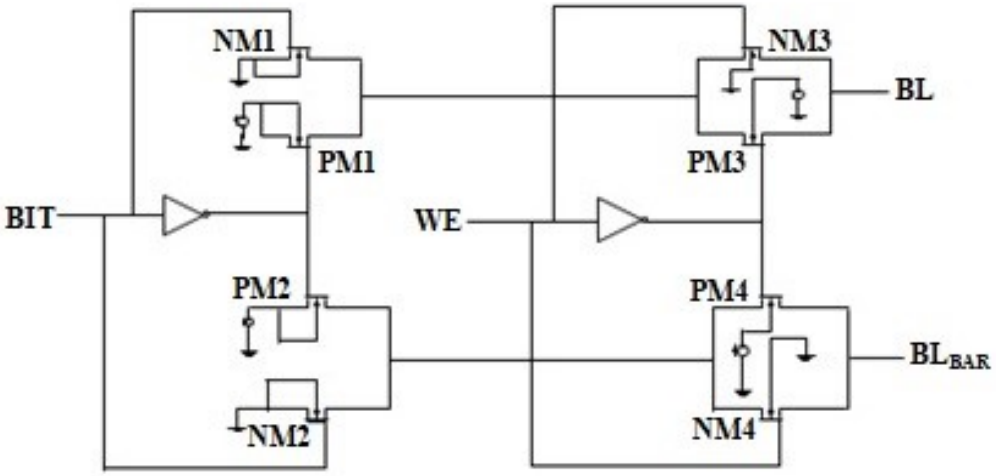
Figure 1: WDC Schematic



2.2 MTCMOS-SRAM

SRAM uses the 6T design in various products. Those in the know refer to the cache memory in computing as "MTCMOS-SRAM." It is a technique for data storage. In this circuit, two inverters and two transistors are wired back-to-back [6]. As can be seen in Figure 2, an MTCMOS-SRAM cell's bit lines can read and write data. Due to its durability and little static power loss, this choice is well-liked. The access transistors on the bit lines can be used when the writing signal is active. Only if the write line is enabled is this possible. As a result, practically everyone nowadays is literate. The 8T design, which comprises two 2T SRAM cells and six 6T SRAM cells, is shown in Figure 3.

Figure 2: Conventional SRAM Circuit Diagram

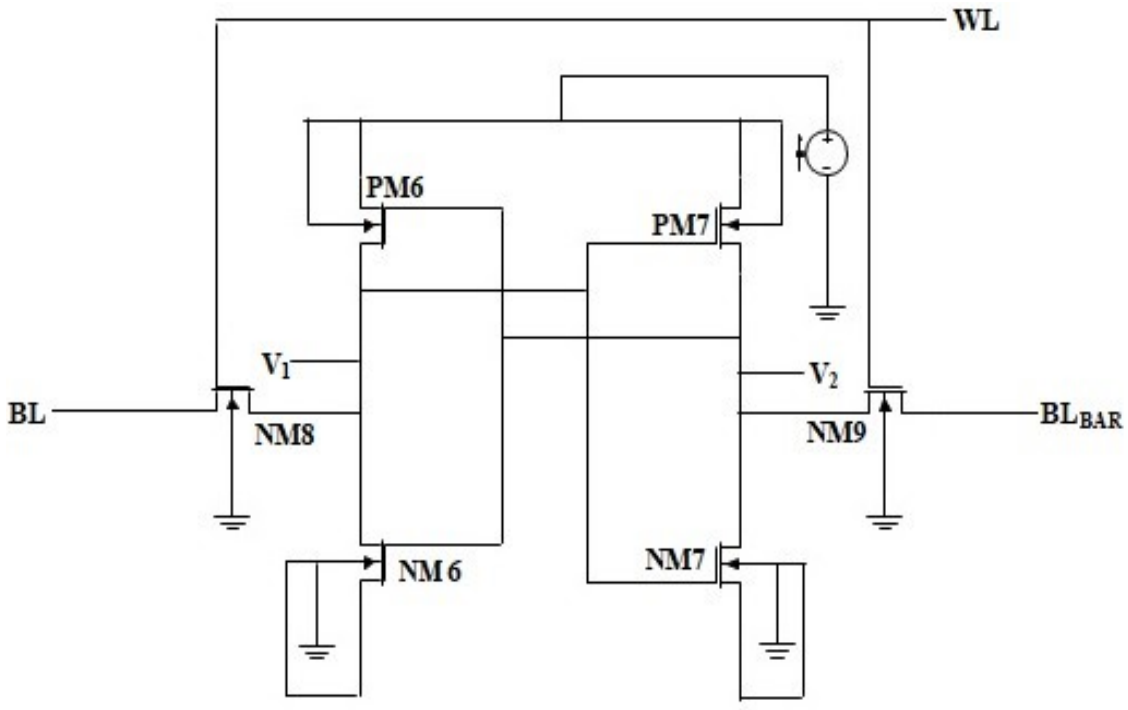


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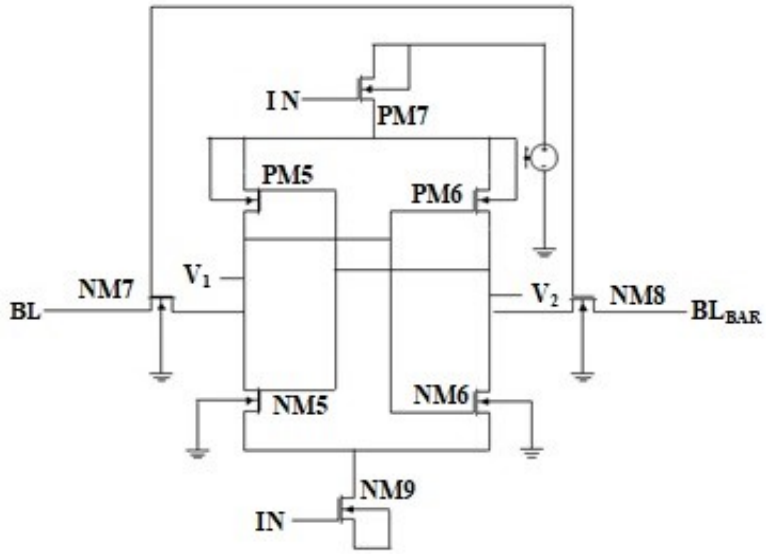
Figure 3: MTCMOS-SRAM

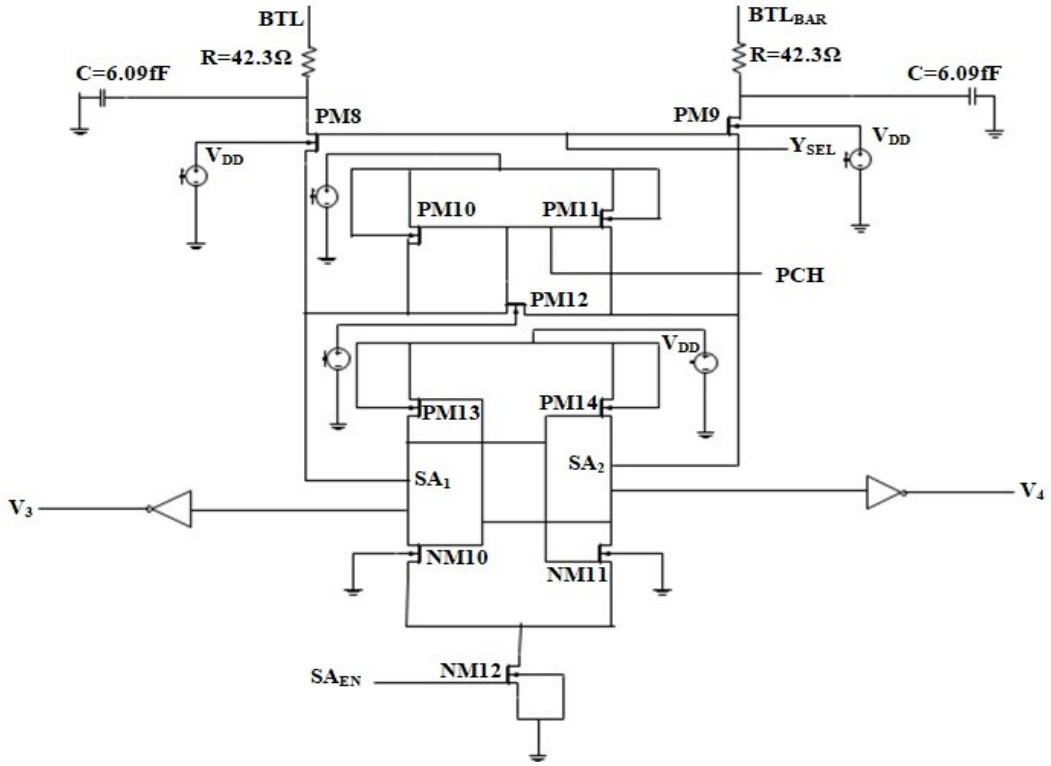


2.3 Sense Amplifiers

2.3.1 VMSA

VMSA takes advantage of differential discharge to calculate the value of the potential difference at the bit capacitance [7]. When WL is turned on, the system's voltage changes noticeably. A positive feedback loop can be utilized to close the voltage difference between the VMSA and Saen to reach full rail voltage. The VMSA's internal wiring is shown in Figure 4.

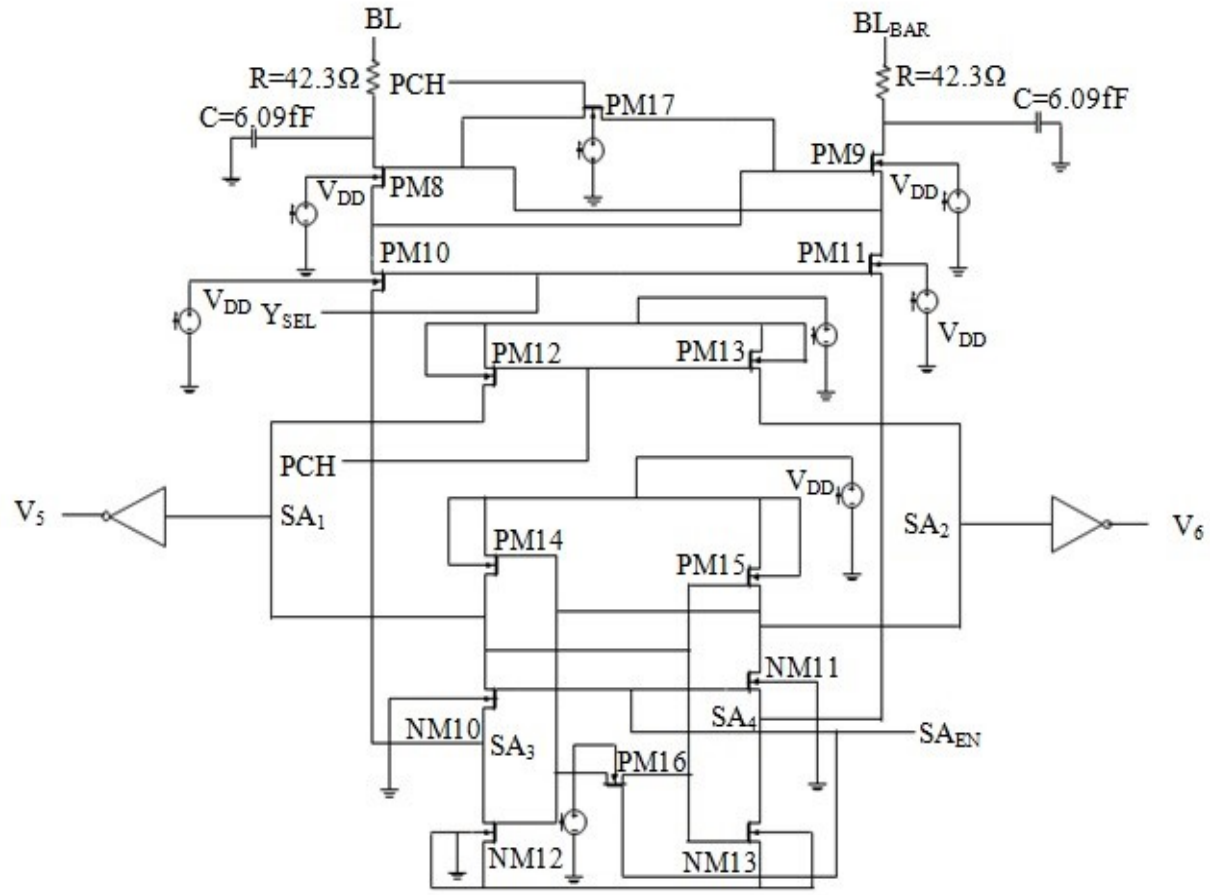
Figure 4: VMSA Schematic



2.3.2 CMSA

CMSA uses differential discharge to calculate the bit capacitance potential difference [8]. When WL is turned on, the system's voltage changes noticeably. Positive feedback loops can convert the full rail voltage of CMSA and Saen [9]. The VMSA's internal wiring is shown in Figure 4.

Figure 5: CMSA Schematic



2.3.3 CTSA

Charges must be moved from high-capacitance (bl) sites to low-capacitance (bl) locations, according to the CTSA. Less energy is used when CTSA is used. The internal wiring of the CTSA is shown in Figure 6. The circuit consists of two different parts. The CG cascade was started at the beginning of the procedure using P1, P3, and P5 (together with P2, P4, and P6). Both the PMOS P1 and P2 Vb values exhibit the same skewness [11]. In the second section, cross-coupled inverters were built using the latches P7 through N11.

2.3.4 VLSA

Figure 7 shows a diagram of a VLSA that is powered by electricity. N1 and N2 parts make comprise a four-piece inverter. When all of these parts are combined, inverters are produced. An inverter converts the bit line (bl) output into a full swing [10,11]. Bit lines are the channels through which electricity enters the circuit. Electrical designs might change if the spacing between input bit lines at different circuit nodes is changed.

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Figure 6: CTSA Schematic

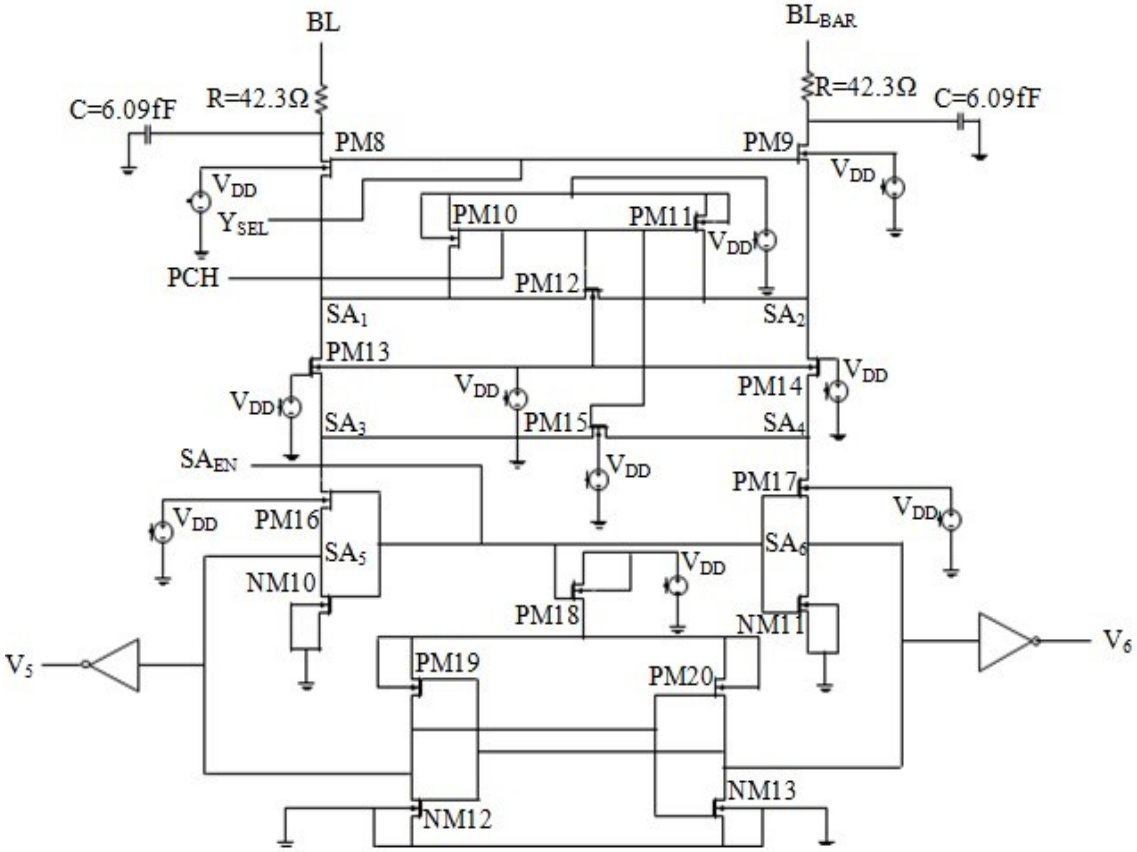
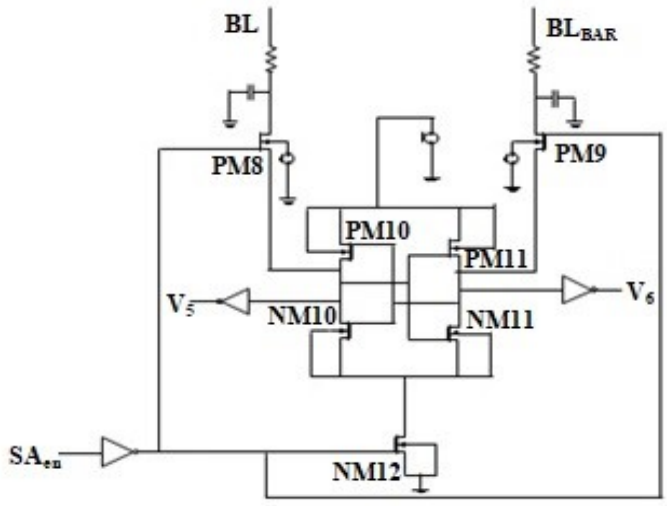


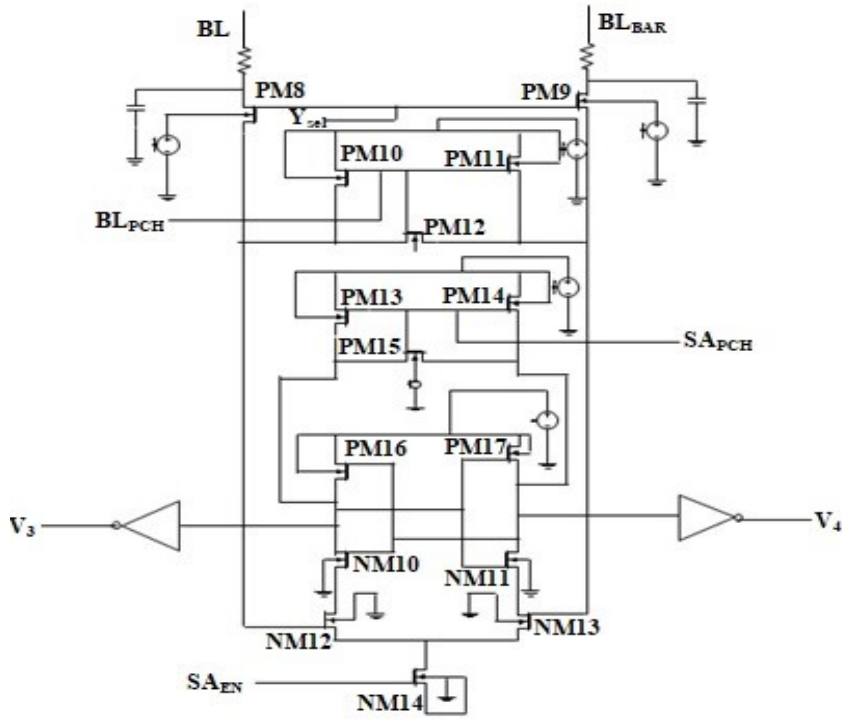
Figure 7: VLSA Schematic



2.3.5 CLSA

Due to its capacity to eliminate energy waste organically and its low electricity consumption, CLSA is a great choice for customers (Fig. 8). The modifications made to the bit line (bl) throughout the read cycle are recorded in the cell [12]. For instance, the N1 and BLB gates of the tree are used to link the two branches together. The latch circuit's two N-mos control the current flow.

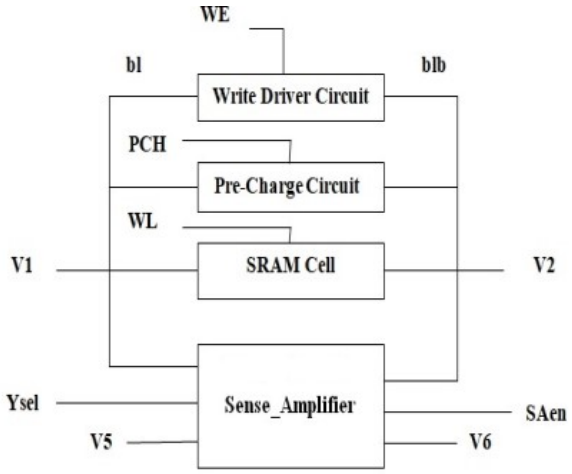
Figure 8: CLSA Schematic



3.0 Analysis of Result

Figure 9 [13] depicts the Single-Bit MTCMOS Cache Memory using SRAM and the CTSA.

Figure 9: Block Structure of Single-Bit MTCMOS Cache Memory Architecture



The cache memory architecture comprises the CTSA, a sensing amplifier, a WDC, a PCH circuit, an MTCMOS-SRAM cell, and other parts. Users can then review the evaluation's findings in the table [14].

In Figure 10, one-bit cache memory is visible. An implementation using one bit. The output of the WDC is connected to the bit lines of the SRAM cell to receive it. The O/p is written to and stored in a memory cell whenever the write line is used.

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Figure 10: Circuit Diagram of MTCMOS CACHE MEMORY Architecture

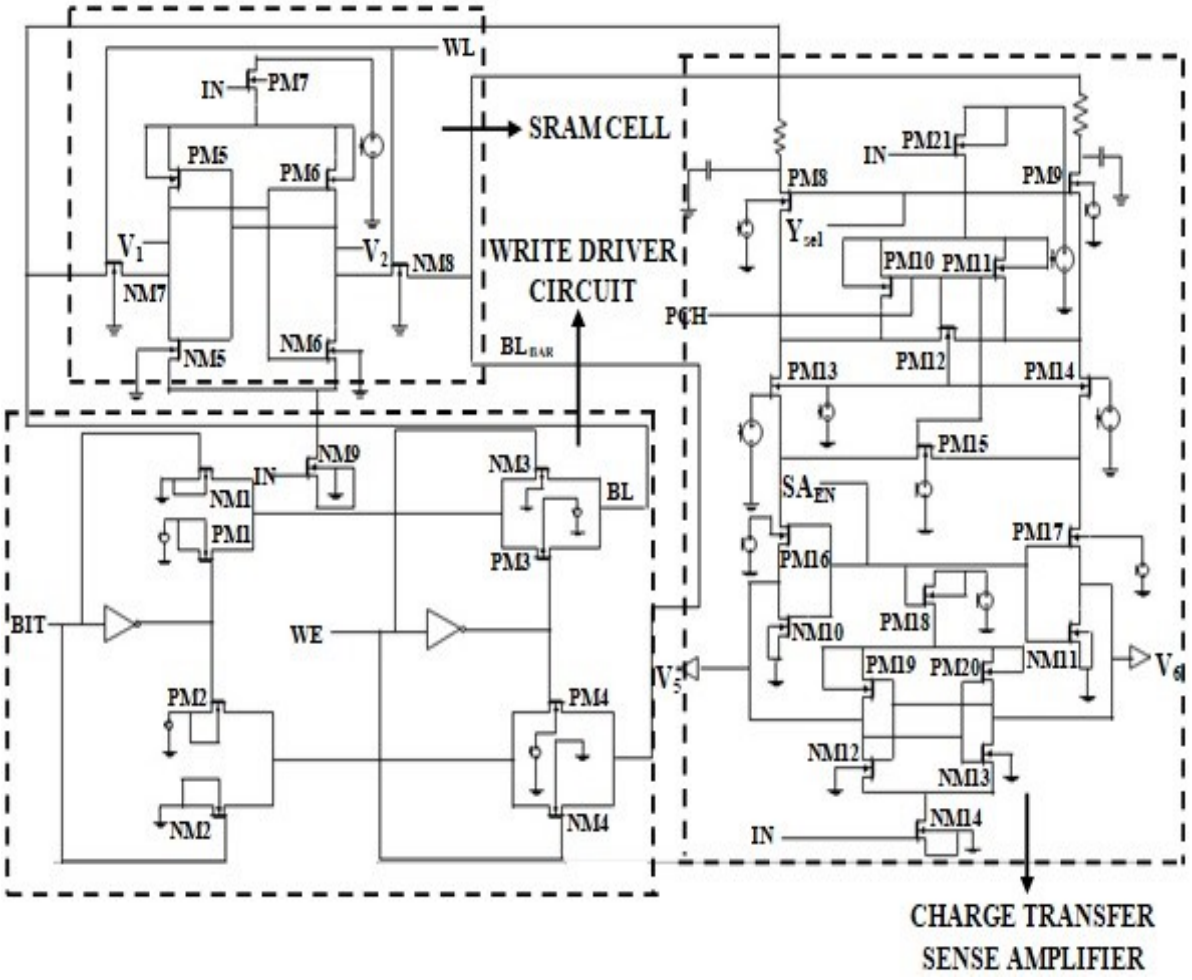
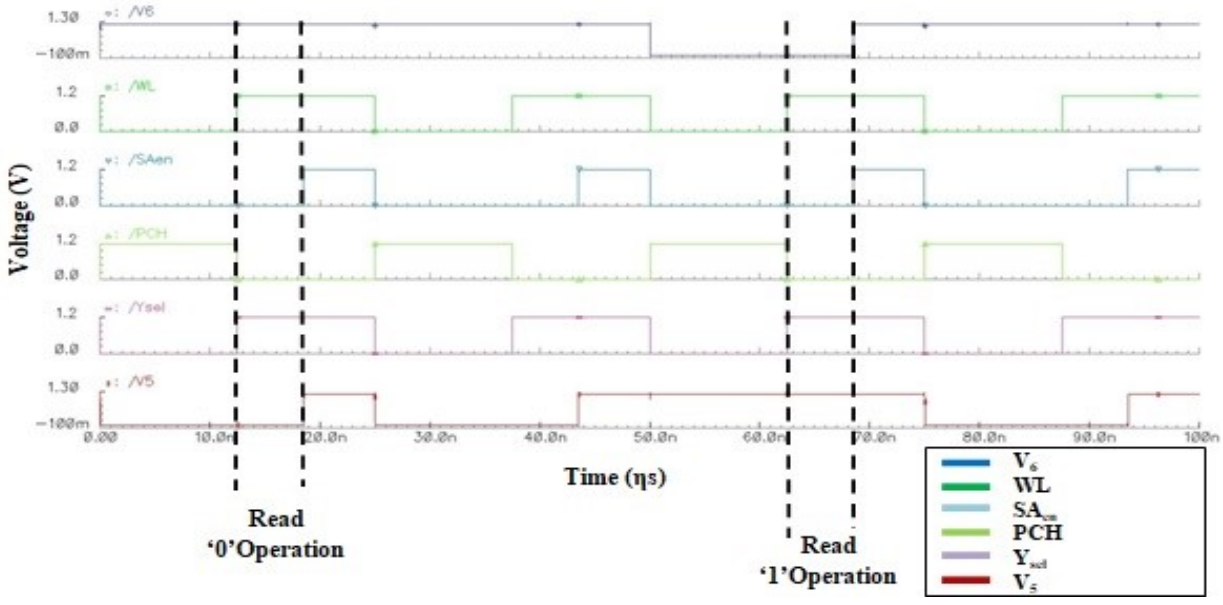


Figure 11: Output Waveform of MTCMOS Cache Memory Architecture



The first table displays the sensing amplifier's power dissipation. Table 2 data demonstrates the various strategies utilized to prevent SRAM from leaking. As shown in Table 3, many sense amplifiers use various techniques to stop leaking.

Table 1: Power Dissipation of Different Techniques Applied to SRAM

S. No.	SRAM with Techniques	Power Consumption
1.	SRAM	.32ηW
2.	MTCMOS SRAM	.176ηW
3.	Sleep Stack SRAM	.213ηW
4.	Sleepy Keeper SRAM	.215ηW
5.	Footer Stacked SRAM	.207ηW

Table 2: Power Dissipation of Different Sense Amplifiers

S. No.	Sense Amplifier	Power Consumption
1.	Voltage Mode Sense Amplifier	100.22 µW
2.	Current Mode Sense Amplifier	70.76µW
3.	Charge Transfer Sense Amplifier	30.23 µW
4.	Voltage Latch Sense Amplifier	620.78 µW
5.	Current Latch Sense Amplifier	310.74 µW

Table 3: Reduced Leakage Power in Sense Amplifier Design

Techniques	VLSA (µW)	CLSA (µW)	CTSA (µW)	VLSA (µW)	CLSA (µW)
Forced-Stack Technique	60.51	6.58	3.25	300.51	110.58
MTCMOS Technique	60.75	6.22	3.85	300.78	70.89
Sleep-Stack Technique	75.48	7.87	3.98	310.10	150.87
Sleepy Keeper Technique	62.78	7.75	3.88	312.52	160.85

VMSA, CMSA, and CTSA are used by the creators of a single-bit cache memory architecture, as indicated in Table 4. It is more likely that this is the case because these three categories of sense amplifiers use substantially less power than the amplifiers in the Tables. The least power-hungry options are the CTSA, MTCMOS-based SRAM, and the CTSA. As a result, an architecture using all of these parts was created using MTCMOS technology. The new layout in Table 4 cuts electricity usage by 98–99%. The term "MTCMOS cache memory" refers to the complete device.

Table 4: Cache memory consumes power with different sense amplifiers

Architecture	Power Consumption
MTCMOS-SRAM with VMSA	266.821 µW
MTCMOS-SRAM SRAM with CMSA	274.296 µW
MTCMOS-SRAM SRAM with CTSA	231.293 µW

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Table 5: Conclusion of all Tables using Different Techniques over Architecture

SRAM with CTSA power consumption in-memory Architecture	Modified SRAM Power Consumption using CTSA in Memory Architecture	SRAM Power Consumption in Memory Architecture with Modified CTSA	Memory architecture Power Consumption of Modified SRAM with Modified CTSA
240μW	12 μW	122 μW	3.00×10^{-3}

4.0 Conclusion

Both MTCMOS CTSA and MTCMOS SRAM were used for the MTCMOS cache. Less power is used by the MTCMOS-CTSA cache memory design than in other comparable systems. Typical MTCMOS circuits consume between 75 and 76 percent less energy than circuits without it. Power consumption can be decreased by 98 to 99 percent with the MTCMOS cache memory architecture. The MTCMOS cache memory was created using several of these creative methods.

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