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Evaluation of the Core Processor Cache Memory Architecture's Performance

Anurag Shrivastava and Mohan Gupta***

ABSTRACT

In this study, memory architectures for single-bit caches are studied. Voltage differential sense amplifiers and charge transfer differential sense amplifiers are used to study a six-transistor static random-access memory. In a single-bit, six-transistor static random-access memory, it has been demonstrated that the voltage differential sensing amplifier uses the least power.

Keywords: *Six Transistor Static Random Access Memory Cell (STSRAMC); Voltage Differential Sense Amplifier (VDSA); Charge Transfer Differential Sense Amplifier (CTDSA); A Sense Amplifier (SA); Write Driver Circuit (WDC); Cache Memory Design for Single Bit Architecture (CMDSBA).*

1.0 Introduction

As the VLSI industry grows, batteries and built-in systems are becoming more crucial. Due to its significance in memory design, the memory cache takes up 60–70% of the chip's surface [1,2]. When more chips are added, the CPU's speed falls. With every million extra transistors, there are more single-chip failures. The group building VLSI systems now have access to a memory circuit that transfers data slowly and with little power. The sensory amplifier is the central theme of this project. Cache memories presently occupy more than half of the transistors in high-performance microprocessors, and this proportion is anticipated to increase [3,4]. Due to its performance in noisy environments, STSRAMC stock is frequently used to replace these chips. To maximize efficiency, several powerful CPUs with low power requirements were considered. Due to its small size and an adequate number of memory cells, the STSRAMC is the ideal memory device [5-7]. With speedier and more potent machinery, work will be more productive. SA, a critical component, is required by all high-frequency STSRAMC memory blocks. The SA setup directly affects memory access times and power usage. SA must be present for a system to store data in memory. By shortening the distance between memory cells and the logic circuit, the SA saves energy [8–10].

2.0 Single Bit Cache Memory Design

Figures 1 and 2 display the design and schematics for one-bit cache memory. Components of the Single Bit Architecture Cache Memory Design include SA, WDC, and STSRAMC.

2.1 WDC

Figure 3 depicts the WDC. The pre-charging processes exhaust the bit lines once the STSRAMC's write margin is reached.

**Corresponding author; Assistant Professor, Department of Mechanical Engineering, SR Institute of Management and Technology, Lucknow, Uttar Pradesh, India (E-mail: onuda@rediffmail.com)*
***Assistant Professor, Mechanical Engineering, United College of Engineering and Eesearch, Naini, Prayagraj, Uttar Pradesh, India (E-mail: mohanguptaucer@gmail.com)*

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Figure 1: Single Bit STSRAMC VDSA Architecture Schematic

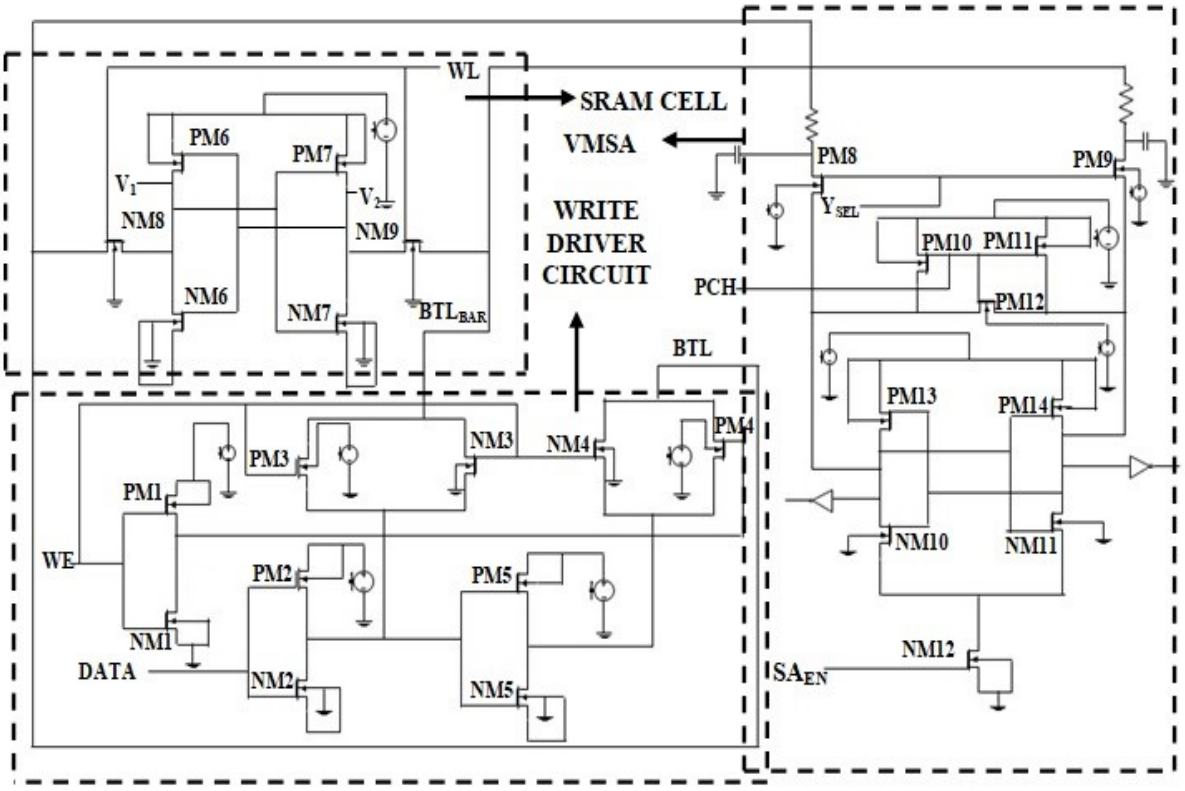


Figure 2: Single Bit STSRAMC CTDSA Schematic

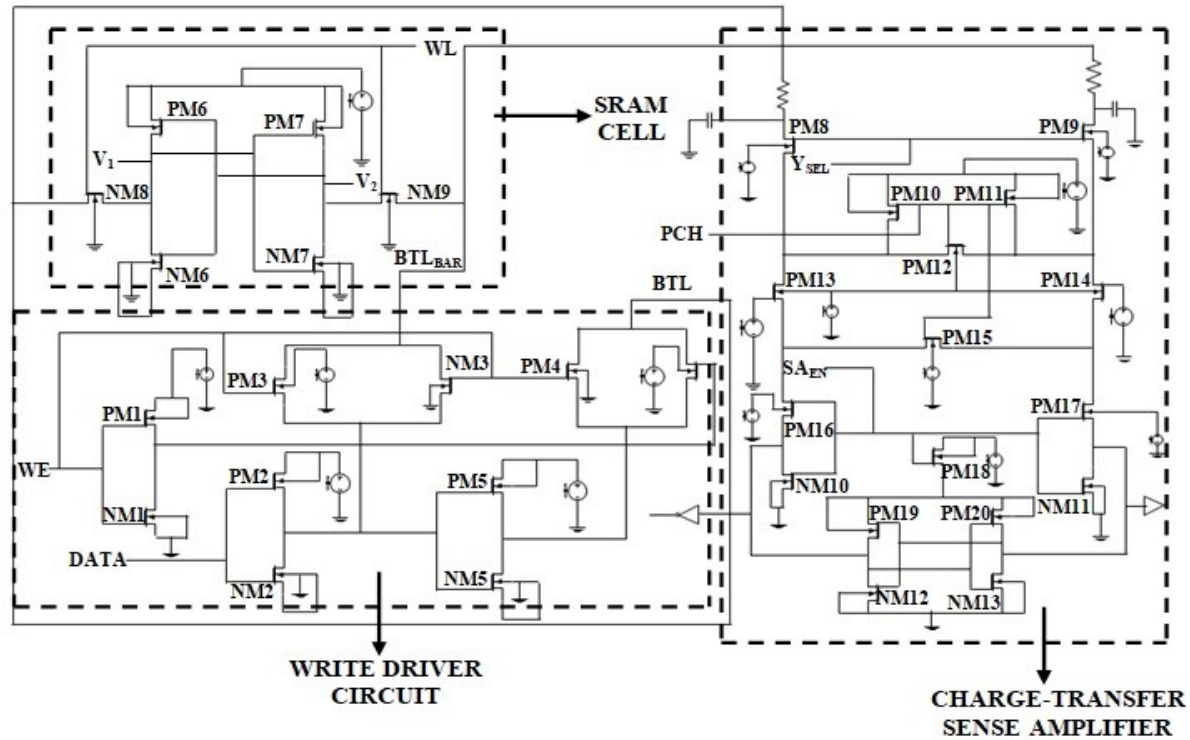
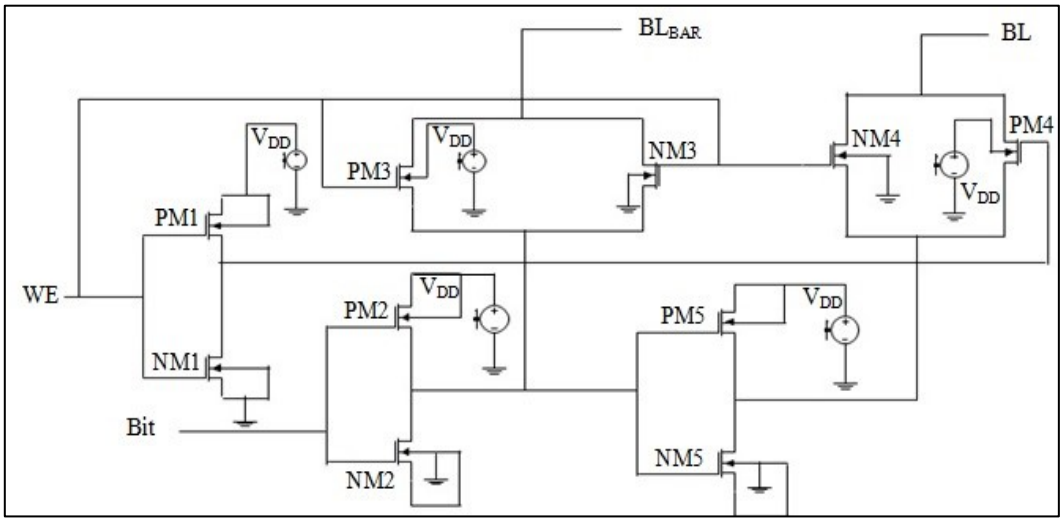


Figure 3: WDC Schematic

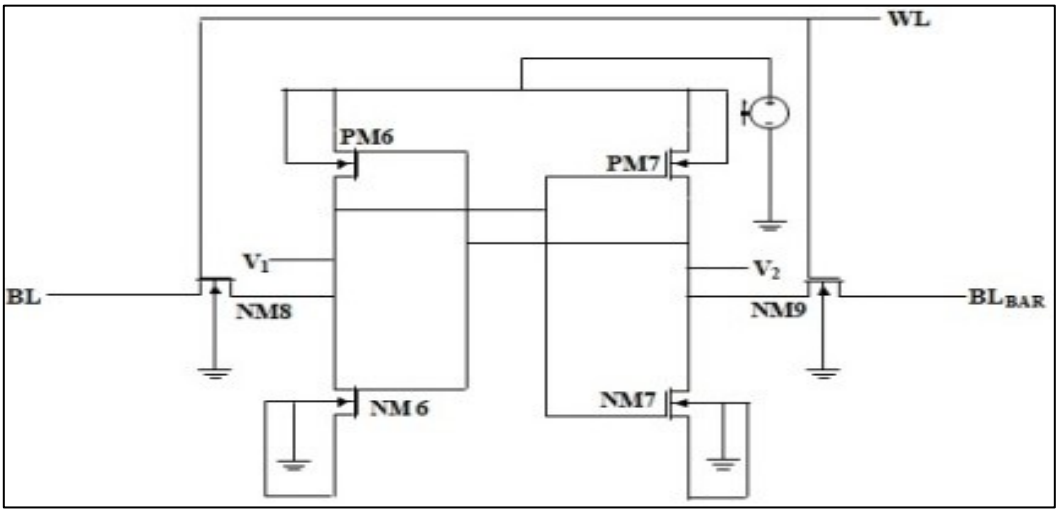


When the WDC is turned on, the bit line drops from pre-charge level to ground potential due to write enable (WE) signals. The PMOS and NMOS each have distinct numbering schemes in the WDC (NM1, NM2, NM3, NM4, and NM5). Pre-charge levels of BTL and BTLBAR are lowered. Depending on the data received, one of the transistors may be PM1 or NM1.

2.2 STSRAMC Working and Schematic

Its use is advantageous for low-power and low-voltage applications. Because each bit stays in its circuit with bistable latching, testing is made simpler. Two pull-up transistors (PM6 and PM7) and two pull-down transistors (PM7 and PM8) are shown in Figure 4 as the STSRAMC circuit (NM6 and NM7). The increasing number of bit lines results in more noise being produced. The output voltage of differential circuits is calculated from the magnitude of the output voltage variation. As long as the electricity is on, a value of 0 or 1 is kept. The size of the transistor has an impact on the STSRAMC architecture's performance.

Figure 4: STSRAMC Schematic



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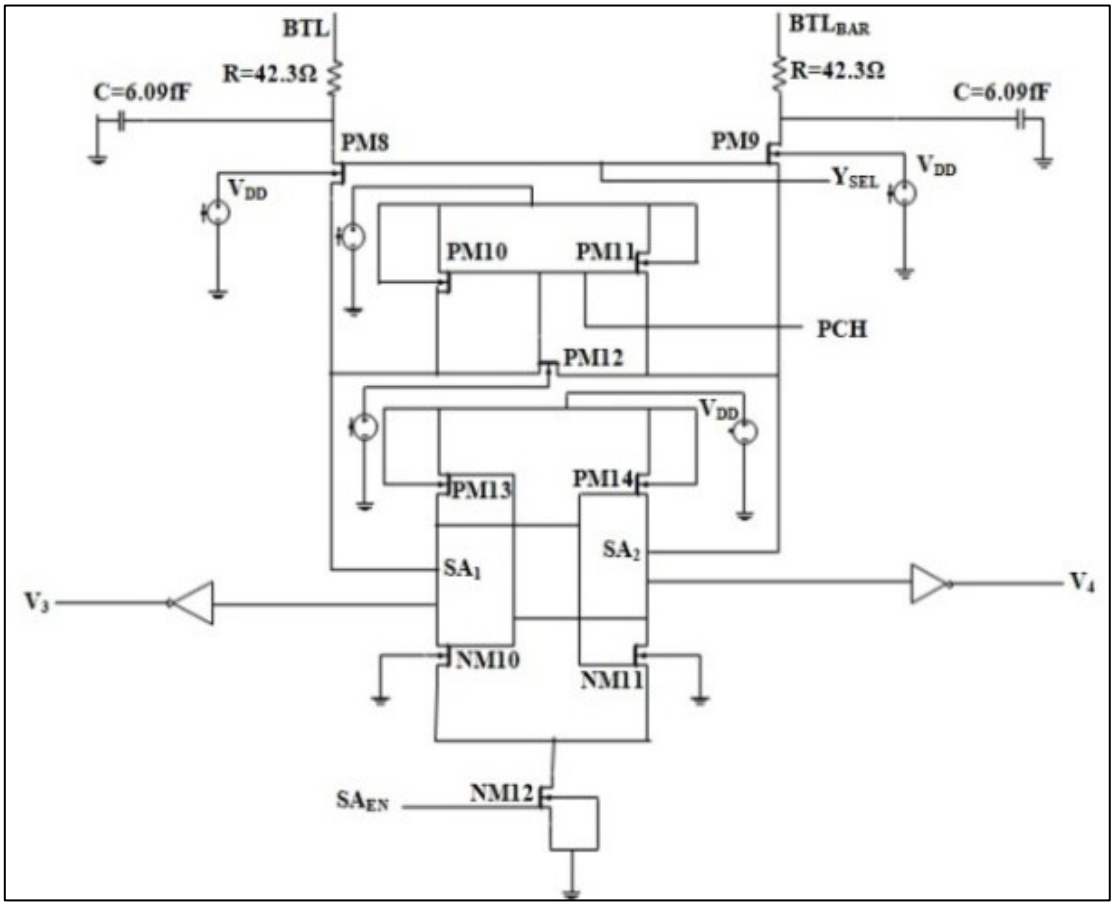
2.3 Sense Amplifier's (SA) Working

The SA improves the minor analog voltage differential between read-access bit lines. The output is digital and single-ended. Bit lines that are longer and wider use more energy and take longer to clean.

2.3.1 VDSA

Everything users need to get started with differential sensing is in a small package. Single-ended inputs and outputs are necessary for differential amplifiers that operate at low signal levels [11]. The noise that makes an amplifier inefficient can be reduced while the difference between two signals can be increased. In memory, a basic differential voltage amplifier is used. These have a significant counterbalance in terms of electricity use. Figure 5 shows a picture of the VDSA.

Figure 5: VDSA Schematic

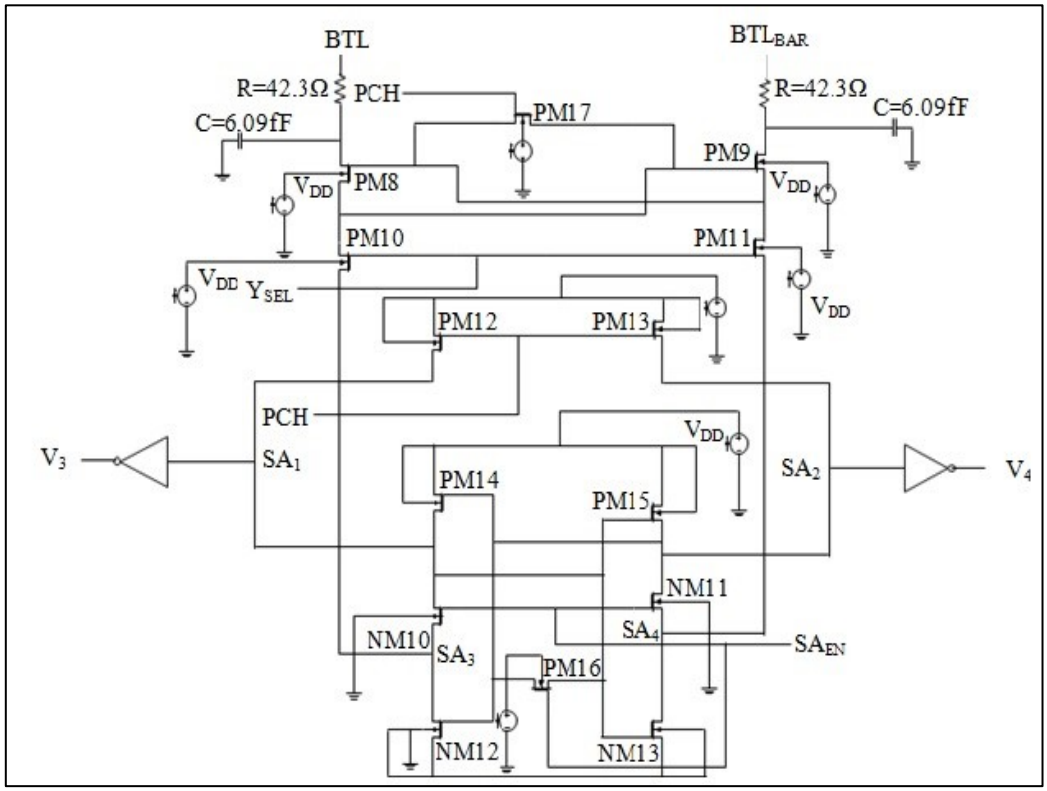


2.3.2 CTDSA Working and Schematic

A charge is transferred from high-capacity bit lines to low-capacity amplifier output nodes, which spreads it across the CTDSA [12,13].

Figure 6 shows that CTDSA uses less energy and has a smaller voltage swing compared to bit lines. The electricity required stays the same even when the processing speed is raised. If this little capacitive element makes the capacitive element's voltage vary more wildly, the voltage might increase.

Figure 6: CTDSA Schematic



3.0 Analysis of Results and Discussion

Figure 7 shows the output of the WDC. Four wires exit and enter in addition to the article (WE, Bit, BTL, and BTLBAR). The waveform was produced by the STSRAMC when holding and writing, as seen in Figure 8. The VDSA and CTDSA read methods use SAEN=high, and WL=high read parameters, as illustrated in Figures 9 and 10.

Figure 7: WDC Output Waveform

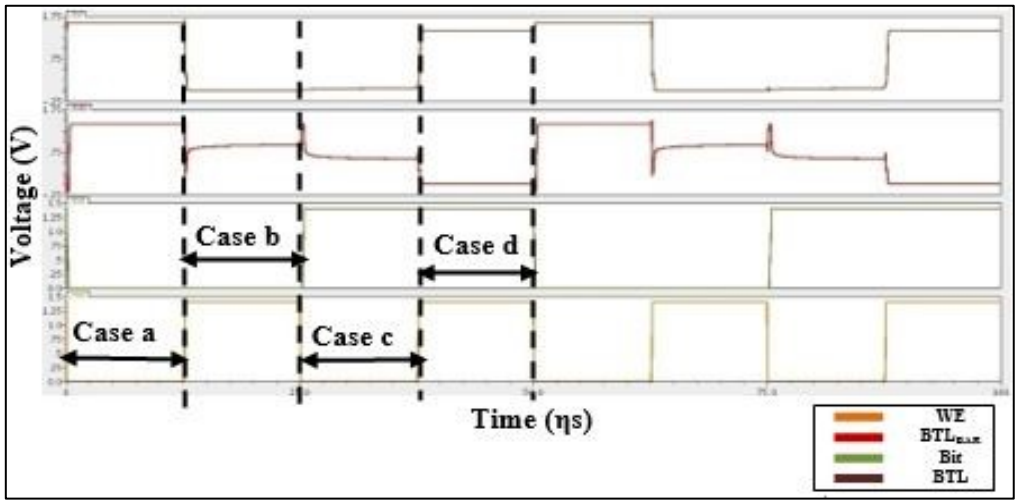


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Figure 8: STSRAMC O/P

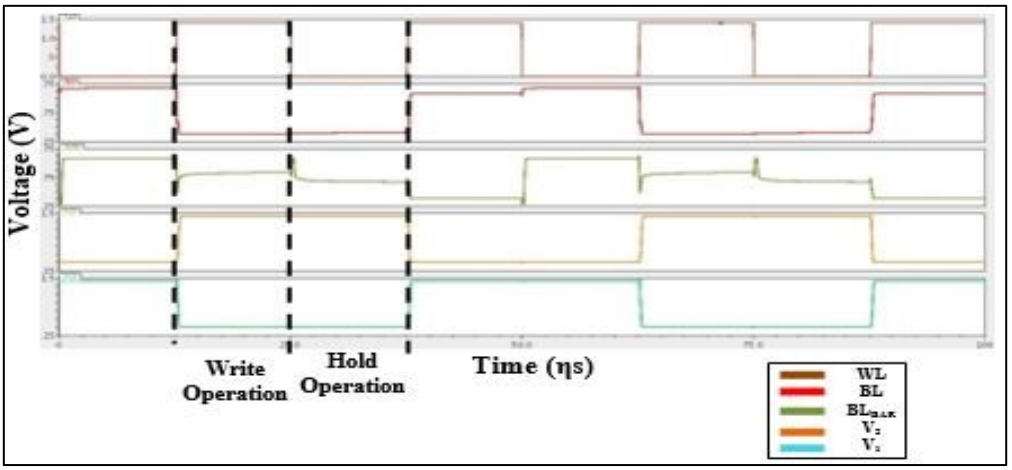

Figure 9: VDSA O/P

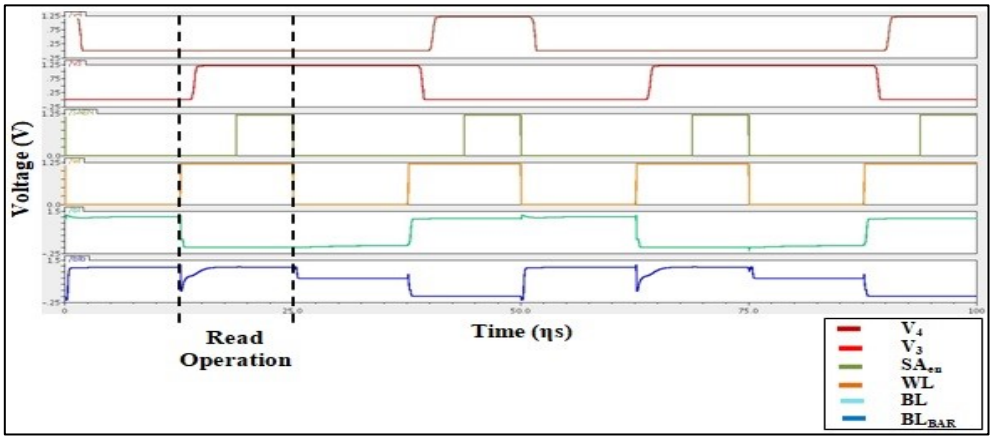

Figure 10: CTDSA Output Waveform

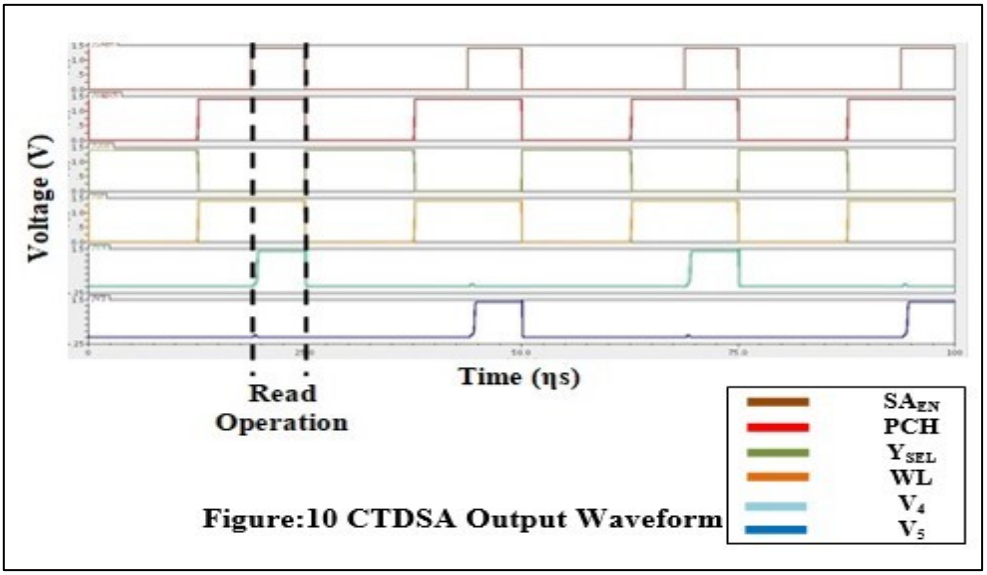

Figure:10 CTDSA Output Waveform

Table 1: Comparison of Single Bit STSRAMC and VDSA Architecture Parameters

S.No.	Parameters	Single Bit STSRAMC VDSA Architecture		
		Dealy in Sensing	Number of Transistors	Consumption of Power
1.	R=42.3Ω	23.23ηs	34	22.52μW
2.	R=42.3KΩ	23.23ηs	34	20.63μW

Resistance does not impact a circuit's size, effectiveness, or speed, as illustrated in Tables 1 and 2. With this equation, power consumption and resistance are inversely related.

Table 2: Comparison of Single Bit STSRAMC and CTDSA Architecture Parameters

S.No.	Parameters	Single Bit STSRAMC CTDSA Architecture		
		Delay in Sensing	Number of Transistors	Consumption of Power
1.	R=42.3Ω	23.23 ηs	40	52.85μW
2.	R=42.3KΩ	23.23 ηs	40	50.56μW

4.0 Conclusion

This study looks at different resistance values (R) and other features like sensing delay, transistor count, and power consumption to evaluate the performance of various SAs, including voltage differential sense amplifiers and charge transfer differential sense amplifiers.

References

1. Verma, Naveen, and Anantha P. Chandrakasan. "A 65nm 8T sub-Vt SRAM employing sense-amplifier redundancy." 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. IEEE, 2007.

2. Verma, Naveen, and Anantha P. Chandrakasan. "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy." IEEE Journal of Solid-State Circuits 43.1 (2008): 141-149.

3. Sinha, Manoj, et al. "High-performance and low-voltage sense-amplifier techniques for sub-90nm SRAM." IEEE International [Systems-on-Chip] SOC Conference, 2003. Proceedings. IEEE, 2003.

4. Do, Anh-Tuan et al. "Design and sensitivity analysis of a new current-mode sense amplifier for low-power SRAM." IEEE transactions on extensive scale integration (VLSI) systems 19.2 (2009): 196-204.

5. Seevinck, Evert, Petrus J. van Beers, and Hans Ontrop. "Current-mode techniques for high-speed VLSI circuits with application to a current sense amplifier for CMOS SRAMs." IEEE Journal of Solid-State Circuits 26.4 (1991): 525-536.

Doi: 10.51976/jfsa.211903

6. Chow, Hwang-Cherng, and Shu-Hsien Chang. "High-performance sense amplifier circuit for low power SRAM applications." 2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No. 04CH37512). Vol. 2. IEEE, 2004.

7. Abu-Rahma, Mohamed H., et al. "Characterization of SRAM sense amplifier input offset for yield prediction in 28nm CMOS." 2011 IEEE Custom Integrated Circuits Conference (CICC). IEEE, 2011.

8. Agbo, Innocent, et al. "Integral impact of BTI, PVT variation, and workload on SRAM sense amplifier." IEEE Transactions on Very Large-Scale Integration (VLSI) Systems 25.4 (2017): 1444-1454.

9. Kobayashi, Tsuguo, et al. "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture." IEICE transactions on electronics 76.5 (1993): 863-867.

10. Wicht, Bernhard, Thomas Nirschl, and Doris Schmitt-Landsiedel. "Yield and speed optimization of a latch-type voltage sense amplifier." IEEE Journal of Solid-State Circuits 39.7 (2004): 1148-1158.

11. Agrawal, Reeya, and Vinay Kumar Tomar. "Analysis of Low Power Reduction Techniques on Cache (SRAM) Memory." 2018 9th International Conference on Computing, Communication, and Networking Technologies (ICCCNT). IEEE, 2018.

12. Agrawal, Reeya, and V. K. Tomar. "Implementation and Analysis of Low Power Reduction Techniques in Sense Amplifier." 2018 Second International Conference on Electronics, Communication and Aerospace Technology (ICECA). IEEE, 2018.

13. Agrawal, Reeya, and V. K. Tomar. "Analysis of Cache (SRAM) Memory for Core i™ 7 Processor." 2018 9th International Conference on Computing, Communication, and Networking Technologies (ICCCNT). IEEE, 2018.