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Topology Using Cascade Multilevel Inverters with Minimal Switches

Chandra Shekher Giri and Utkarsh Singh***

ABSTRACT

Since their inception in the late 1990s, multilevel inverters have experienced a number of modifications, some of which include novel topologies, control mechanisms, and modulation procedures. The most important reason for making such modifications was to reduce the burden on the system by getting rid of part of the switching components, while at the same time enhancing the resolution of the output voltage. In this research, a multilevel inverter and its ability to generate an output voltage spectrum consisting of seventeen discrete levels is investigated. The multilevel inverter in question makes use of eight switching devices. This configuration generates very little harmonic distortion because to the application of a multi-carrier pulse width modulation technique.

Keywords: *Cascade Multilevel Inverter (CMI); Semi-conductors; Level Shifted; Total Harmonic Distortion (THD); In Phase Disposition (IPD).*

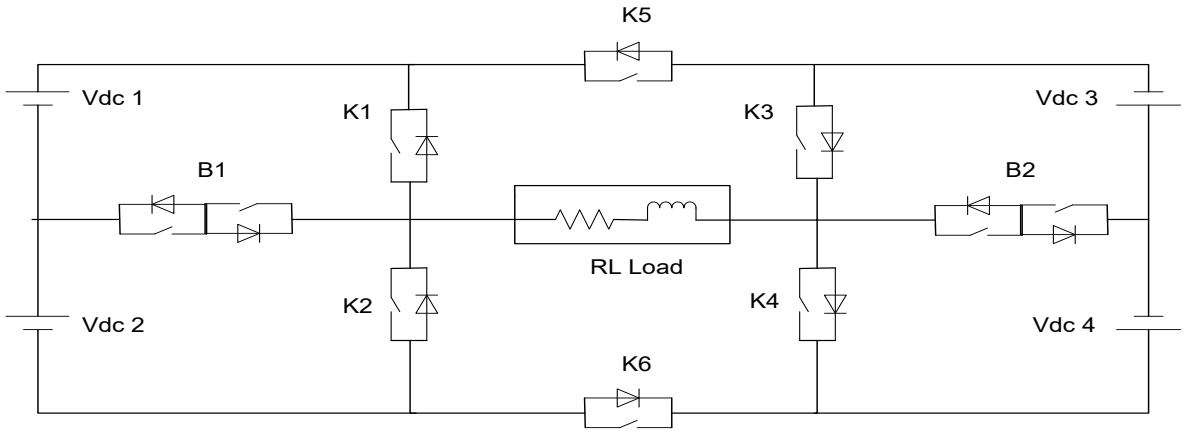
1.0 Introduction

By adding cells in a cascade pattern, a multilevel inverter is able to provide an output voltage at a higher level and a waveform that is approximately sinusoidal [1]. As compared to the other two primary multilevel inverter topologies—the diode-clamped H-bridge and the flying-capacitor topologies—the cascade H-bridge has many advantages over its counterparts [2]. Typically, a single dc source and two switches are used in each leg of a cascade multilevel inverter. When all of the dc sources have the same magnitude, the resulting configuration is called a symmetrical configuration, but when they have different magnitudes, the resulting structure is called an asymmetrical configuration [3]. One of the key parameters in determining the price and efficacy of a power converter's cooling system is the converter's loss. While an asymmetrical layout allows for a greater range of voltages to be used in a given circuit, it comes with the significant drawback of putting a heavy load on all of the switches during operation [4].

In order to achieve a greater number of voltage levels, a cascade architecture multilevel inverter requires a greater number of cells (N = 2M+1), where M is the needed number of cells and N is the desired number of voltage levels [5]. As the number of cells in a circuit grows, so does the number of switches linked to it, increasing the complexity of the circuit's design and operation. The modulation approach plays a crucial role in improving the efficiency of the new topology for CMI [6]. This study presents a CMI-based architecture with seventeen levels that uses the multi-channel power-wave management (MCPWM) approach. A CMI-based architecture with a decreased number of switches, as illustrated in fig.1, is used to provide an output voltage with seventeen discrete steps.

**Corresponding author; M. Tech Research Scholar,Department of Civil Engineering, KNIT Sultanpur, Uttar Pradesh, India (E-mail: giri.ucem@gmail.com)*
***Design Engineer, Maxbros Venture India Pvt Ltd (E-mail: utkarsh.vns1122@gmail.com)*

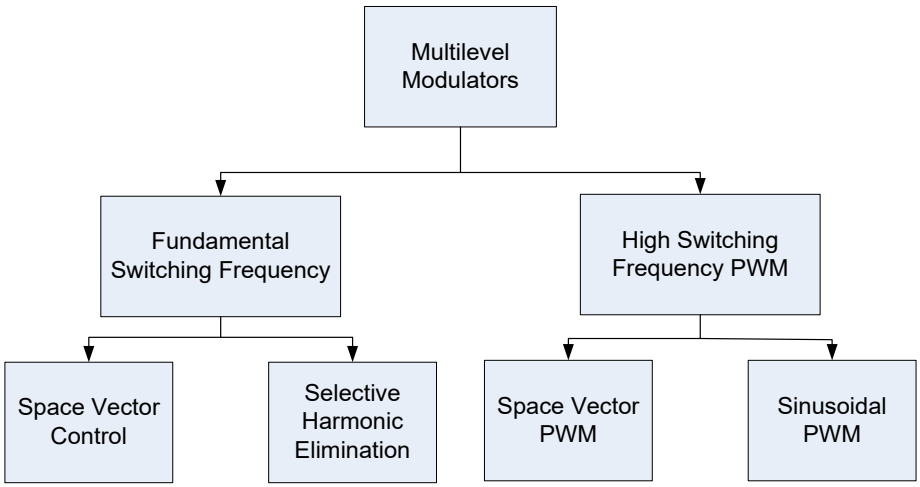
Figure 1: CMI based Topology



2.0 CMI Based Topology with Reduced Switch Count

CMI, with its modular construction, is the most efficient design for multilevel inverters, but it has drawbacks such as increasing the number of switching devices to increase the output voltage levels [7]. In order to address this shortcoming of CMI, a novel topology has been shown in which fewer switches are used than in the conventional cascade architecture of multilevel inverter.

Fig.2: Modulation Techniques Classification for CMI



2.1 Circuit framework for new topology of CMI

As can be seen in Figure 1, this work introduces a cascade multilayer inverter based design that requires fewer switching components. In contrast to the traditional topology, which uses 32 switches to achieve the same number of levels (17), the given design requires just eight. In this circuit, the switches B1 and B2 on the left and right sides are bidirectional, but the six switches K1, K2, K3, K4, K5, and K6 in the middle are unidirectional. All the switches brought about by the inductive load being used have likewise been outfitted with anti-parallel diodes in this topology. Vdc1, Vdc2, Vdc3, and Vdc4 are four different dc sources used at both ends of the circuit. To get seventeen distinct states, an asymmetrical setup is used in which the left and right battery terminals' voltage ratings are maintained distinct. When all four batteries have the same voltage rating, this configuration is called a symmetrical arrangement, and it may provide nine different levels of output voltage.

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2.2 Method of operation for CMI based topology

The operating procedure for the circuitry depicted in Figure 1 is explained in terms of the output voltage levels that must be produced and the quantity of power semi-conducting elements in which various voltage levels are created using the circuit looping approach. This system can provide a maximum voltage of roughly 200 volts. For every voltage level, various switching configurations are activated. To obtain the seventeen levels of output voltage illustrated in table 1 using this design, the circuit must have seventeen switching states.

In both asymmetrical and symmetrical configurations, this configuration was being utilised; in asymmetrical layout, the dc voltage sources on the left end side have common characteristics that are different from the values taken for the dc voltage sources on the right outer end, while in symmetrical configuration, the magnitude of all dc sources is the same. One left end side DC voltage source is included in an asymmetrical layout with three right end side DC voltage sources. The functional differences between symmetrical and asymmetrical CMI setups are summarised in Table 2 below. This table shows the number of DC sources utilised in the CMI-based architecture, the number of output voltages, the number of switching devices, and the maximal output voltage that was achieved.

2.3 Loss calculation Of CMI

It is important to take extra care while creating the switching state of the circuit to ensure that all switches are subjected to an equal amount of voltage stress and that there are an equal proportion of switches in the on condition with each voltage level.

Switching device losses, one of the key components of a power converter that also comprises conduction losses and switching losses, can be used to analyse the functionality of the CMI [8]. Due to the negligibly low current during the off state, turn off losses are typically ignored. To determine conduction losses, multiply the on-state voltage by the on-state current.

Equations (1) and (2) may be used to get the peak and average conduction losses, respectively.

$$p_{on}(t) = |i_c(t)|(V_0 + R_{on}|i_c(t)|) \quad \ldots(1)$$

$$p_{avg} = \frac{1}{2\pi}\int_0^T p_{on}\,(t)dt \quad \ldots(2)$$

The on-state current i_c is related to the threshold voltage V_0 and the equivalent resistance R_{on} of semiconducting devices (t).

Because of the time it takes for switching devices to go from their off to them on states, energy is lost in the form of switching losses. Switching loss is the sum of diode turn-on and turn-off losses, and the latter may be avoided if the former is known. IGBT switching energy dissipation may be broken down into losses during IGBT on, IGBT off, and diode off using equations (3), (4), and (5), respectively.

$$E_{on=\int_{t1}^{t2} v(t)*i(t)dt} \quad \ldots(3)$$

$$E_{off=\int_{t3}^{t4} v(t)*i(t)dt} \quad \ldots(4)$$

$$E_{rr=\int_{t5}^{t6} v_{rr(t)*i_{rr}}(t)dt} \quad \ldots(5)$$

Power converter switching losses are sensitive to load situation, dc link inductance, gate circuit inductance, and temperature.

3.0 Modulation Techniques

Multilevel inverters use a modulation method predicated on the switching frequency of carrier

waves, which may be constant or variable, as illustrated in fig. 2 [9, 10]. It was hypothesised that phase shift carrier modulation would be more effective than SHE. MCPWM is favoured [11] because it provides less THD and a better output waveform, two of the most desirable characteristics of CMI. The output voltage waveform exhibits some degree of harmonics of lower order in the constant switching frequency technique, and it incurs less switching loss than the variable switching frequency approach [12]. It was hypothesised that phase shift carrier modulation would be more effective than SHE when the number of levels was large. Switching state redundancy is another strength of multilevel inverters, since it allows for versatile pattern design of switching, which is essential in space vector modulation systems.

Figure 3: Level-Shifted (IPD) Modulation Pattern Seventeen-Level CMI

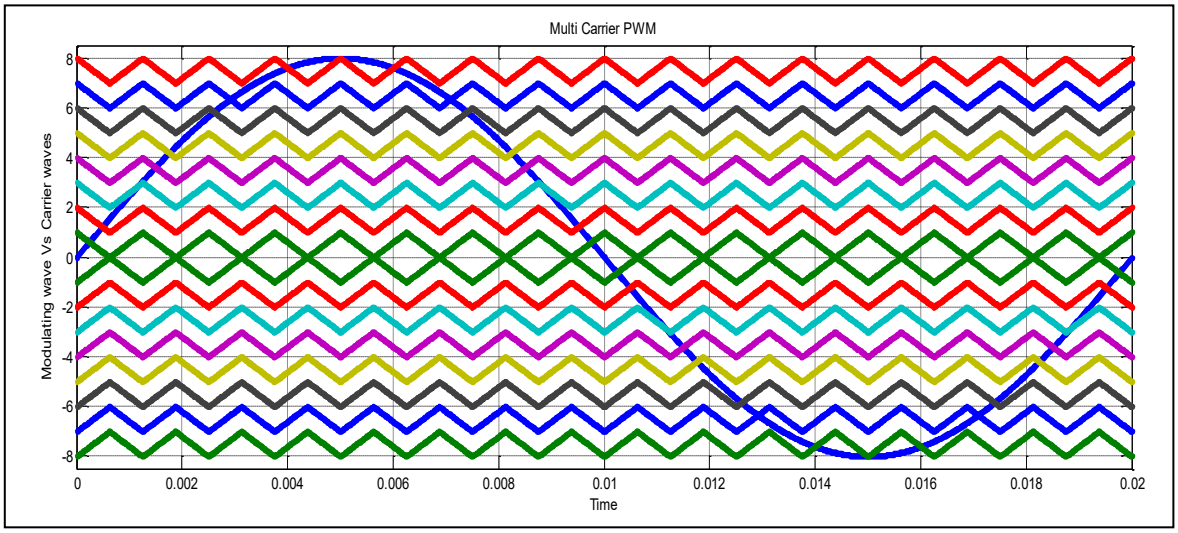

Table 1: Switching States for CMI Based Topology

N_{level}	V_{out}	Switches (ON state)
1	0	K1, K3, K5
2	V_{dc}	K4, K6, B1
3	$2V_{dc}$	K1, K4, K6
4	$3V_{dc}$	K2, K6, B2
5	$4V_{dc}$	K6, B1, B2
6	$5V_{dc}$	K1, K6, B2
7	$6V_{dc}$	K2, K3, K6
8	$7V_{dc}$	K3, K6, B1
9	$8V_{dc}$	K1, K3, K6
10	$-V_{dc}$	K3, K5, B1
11	$-2V_{dc}$	K2, K3, K5
12	$-3V_{dc}$	K1, K5, B2
13	$-4V_{dc}$	K5, B1, B2
14	$-5V_{dc}$	K2, K5, B2
15	$-6V_{dc}$	K1, K4, K5
16	$-7V_{dc}$	K4, K5, B1
17	$-8V_{dc}$	K2, K4, K5

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Table 2: Comparison Between Asymmetrical and Symmetrical Configuration of CMI Based Topology

Configuration	n	N	S_k	Vo
Asymmetrical	4	4n+1= 17	6	200
Symmetrical	4	2n+1= 9	6	100

4.0 Simulation Result

Cascade multilevel inverter based architecture is shown by simulating a multilevel inverter in MATLAB for both asymmetrical and symmetrical configurations (see fig. 1). By using the MCPWM (IPD) approach, as illustrated in fig. 3, this CMI structure may provide seventeen different levels of output voltage for an asymmetrical arrangement, and nine different levels of output voltage for a symmetrical design.

Fig.4: Seventeen-level Output Voltage for Asymmetrical Configuration

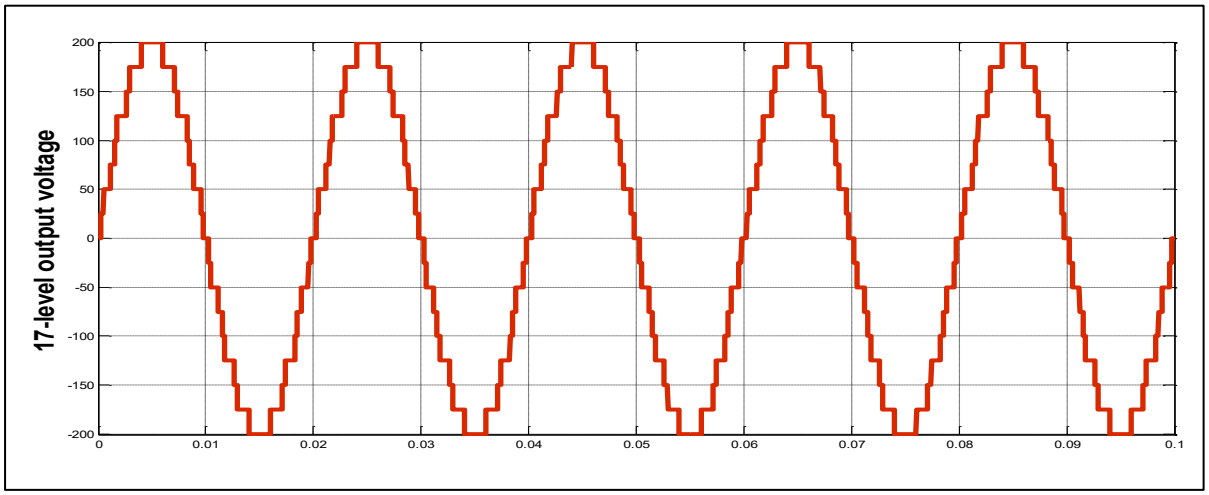
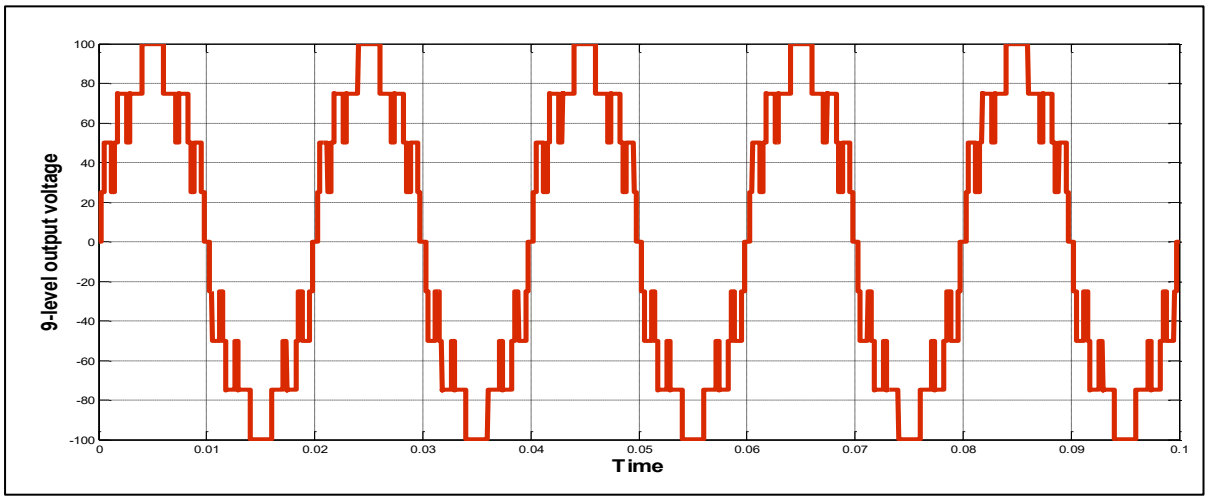


Fig.5: Nine-level Output Voltage for Symmetrical Configuration



Figures 4 and 5 depict the voltage output at various loads and unloadings, with the latter showing nine levels. The highest output voltage of the seventeen settings is 200 volts, with nine settings offering 100 volts. This inverter will be used with a resistive-inductive type load at a frequency of 50 Hz. Fig. 6 displays the voltage and current produced by a seventeen-level inverter when it is fully loaded. Figures 7 and 8 demonstrate that for an inverter with seventeen levels of voltage regulation, the harmonic distortion of the output voltage is 6.25 percent, and for an inverter with nine levels of regulation, it is 21.83 percent.

Figure 6: Output Voltage & Current for Seventeen-level CMI at Loaded Condition

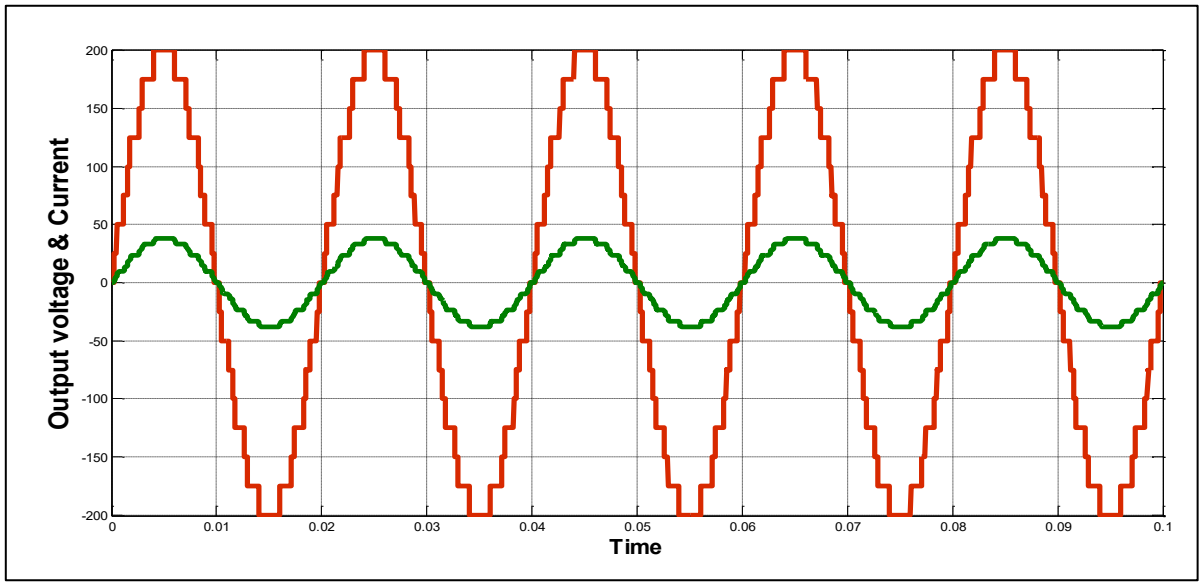


Fig.7: THD Spectra of Output Voltage for Seventeen-level CMI

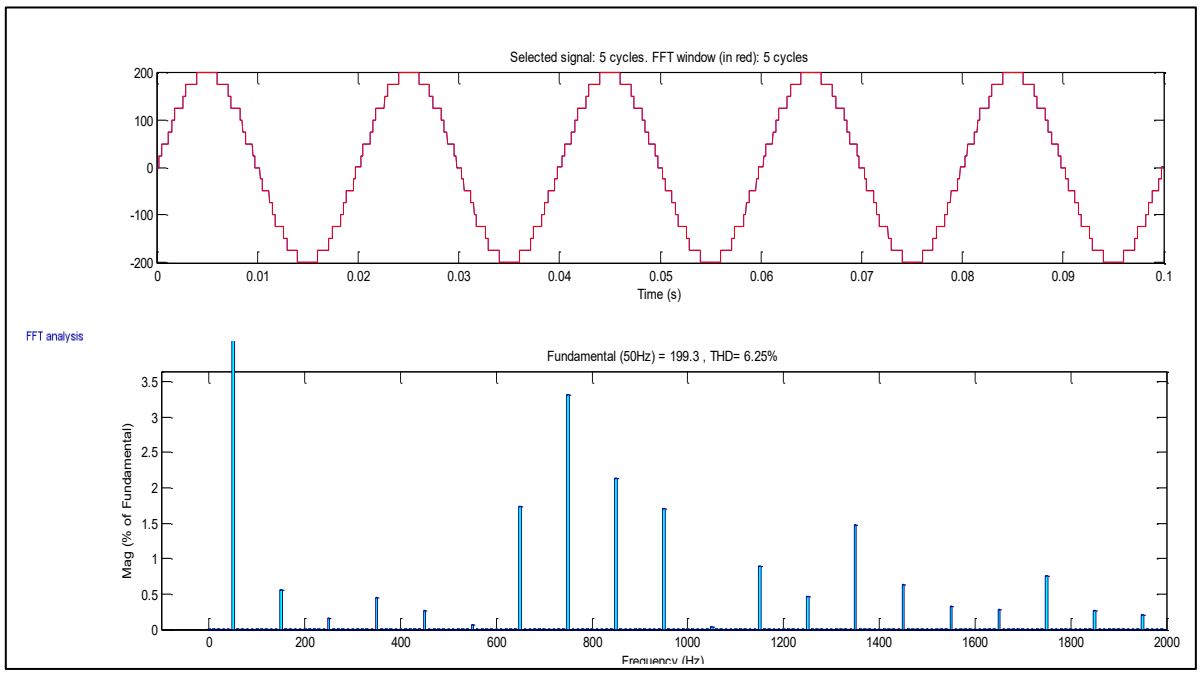
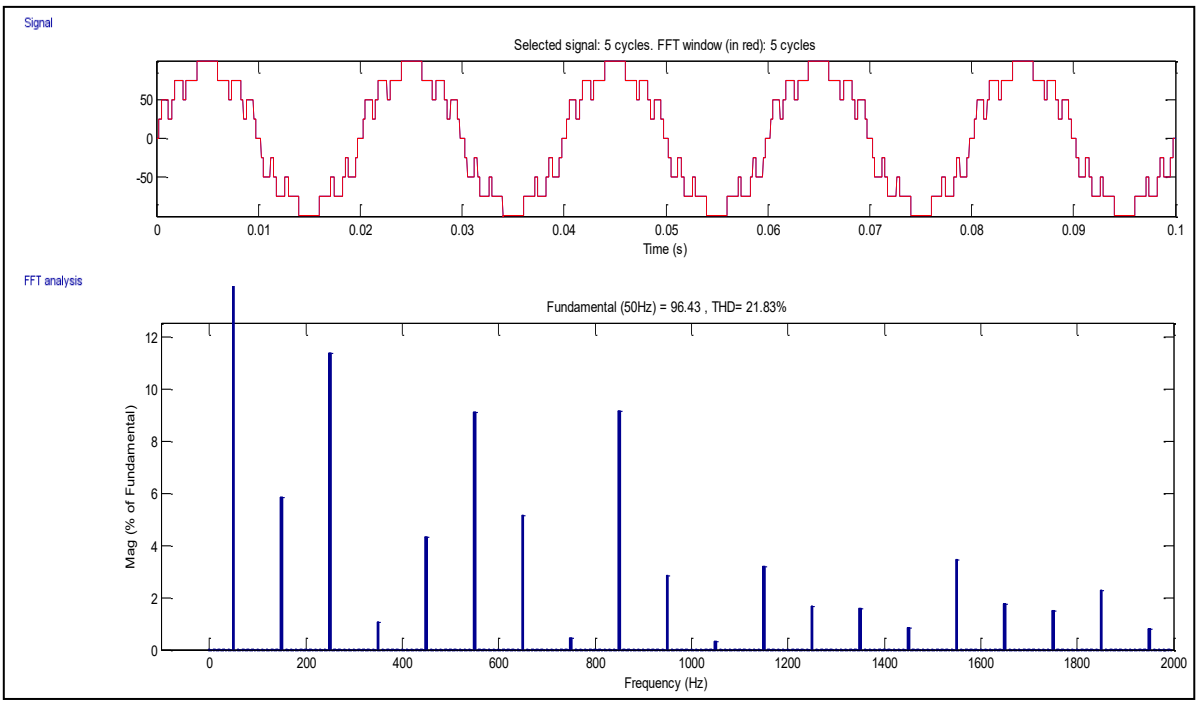


Figure 8: THD Spectra of Output Voltage for Nine-level CMI



5.0 Conclusion

This study uses MATLAB simulation to elaborate on the workings of a multilevel inverter with an arrangement of eight switching devices, two of which are bidirectional and the rest of which are unidirectional. The highest output voltages found in simulation are 200 V for an asymmetrical design and 100 V for a symmetrical one. Harmonic distortions average 6.25 percent with CMI 17, whereas they average 21.83 percent at CMI 9. Here, MCPWM is employed to generate such high voltages.

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